

FIG. 1

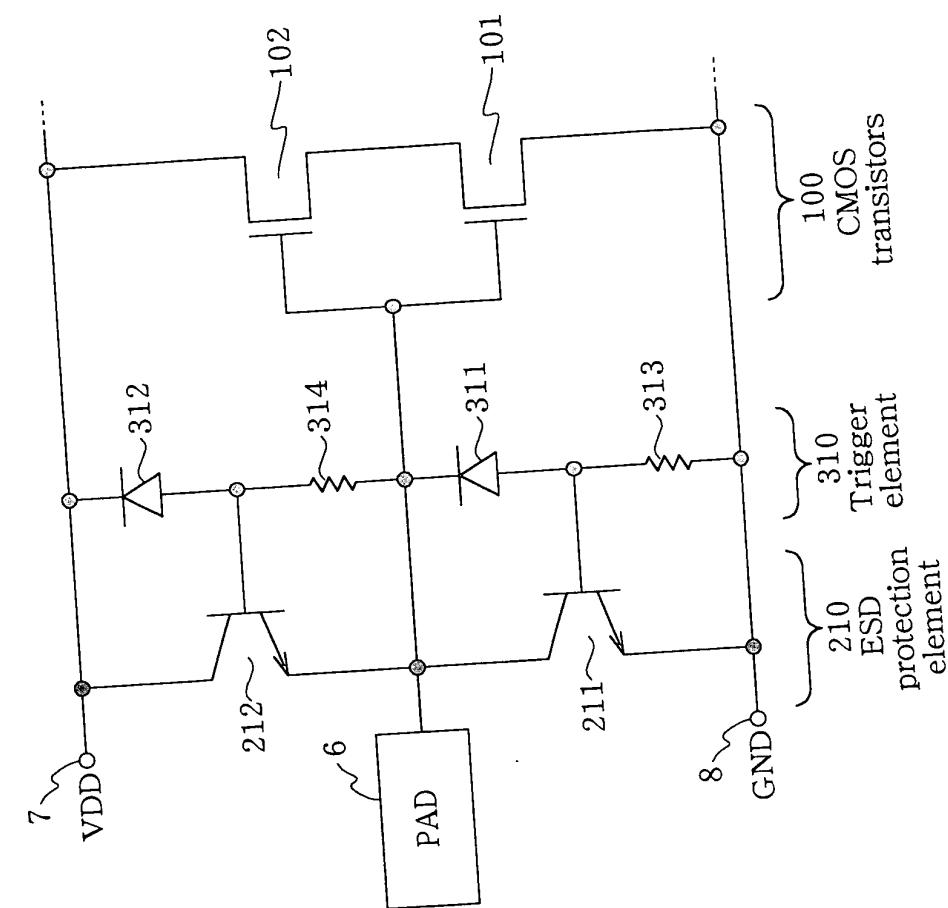


FIG. 2

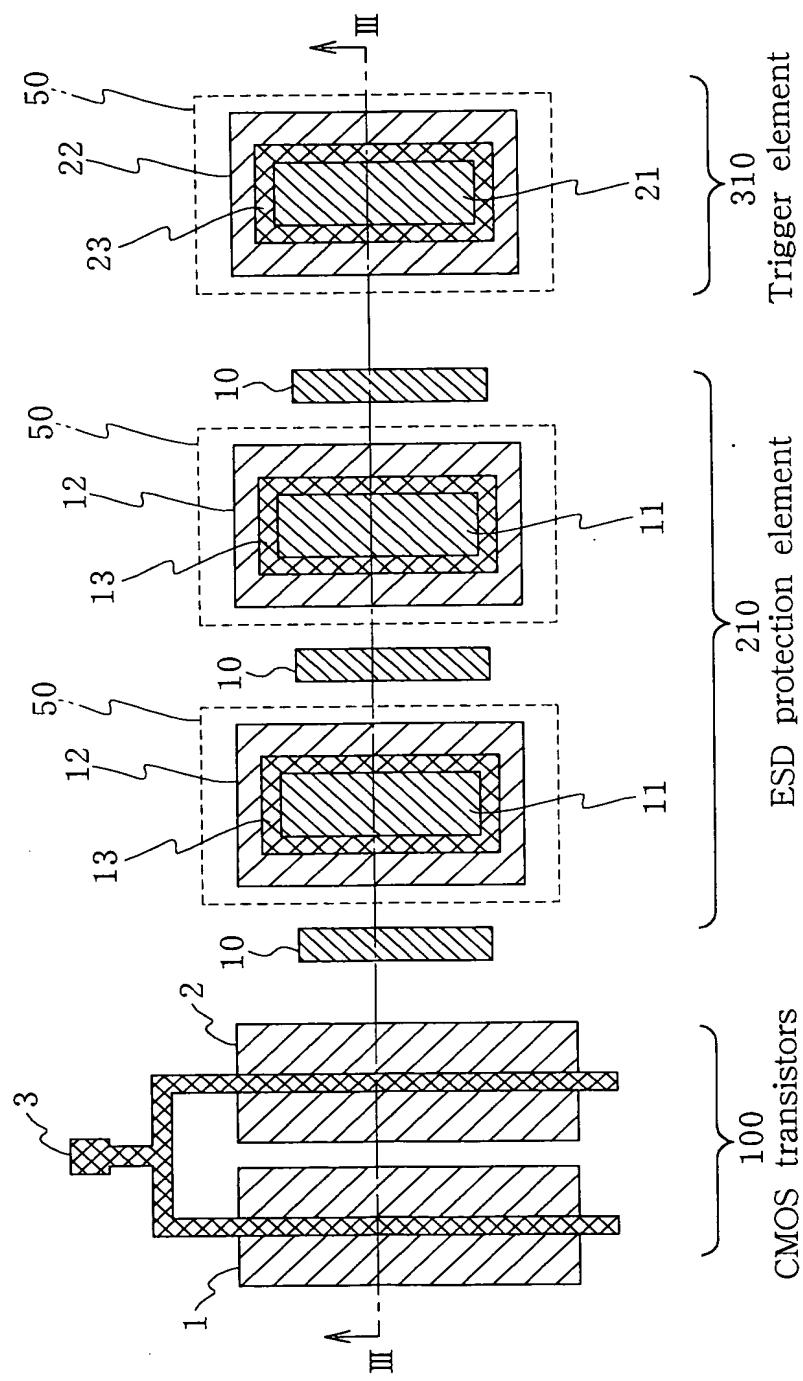


FIG. 3

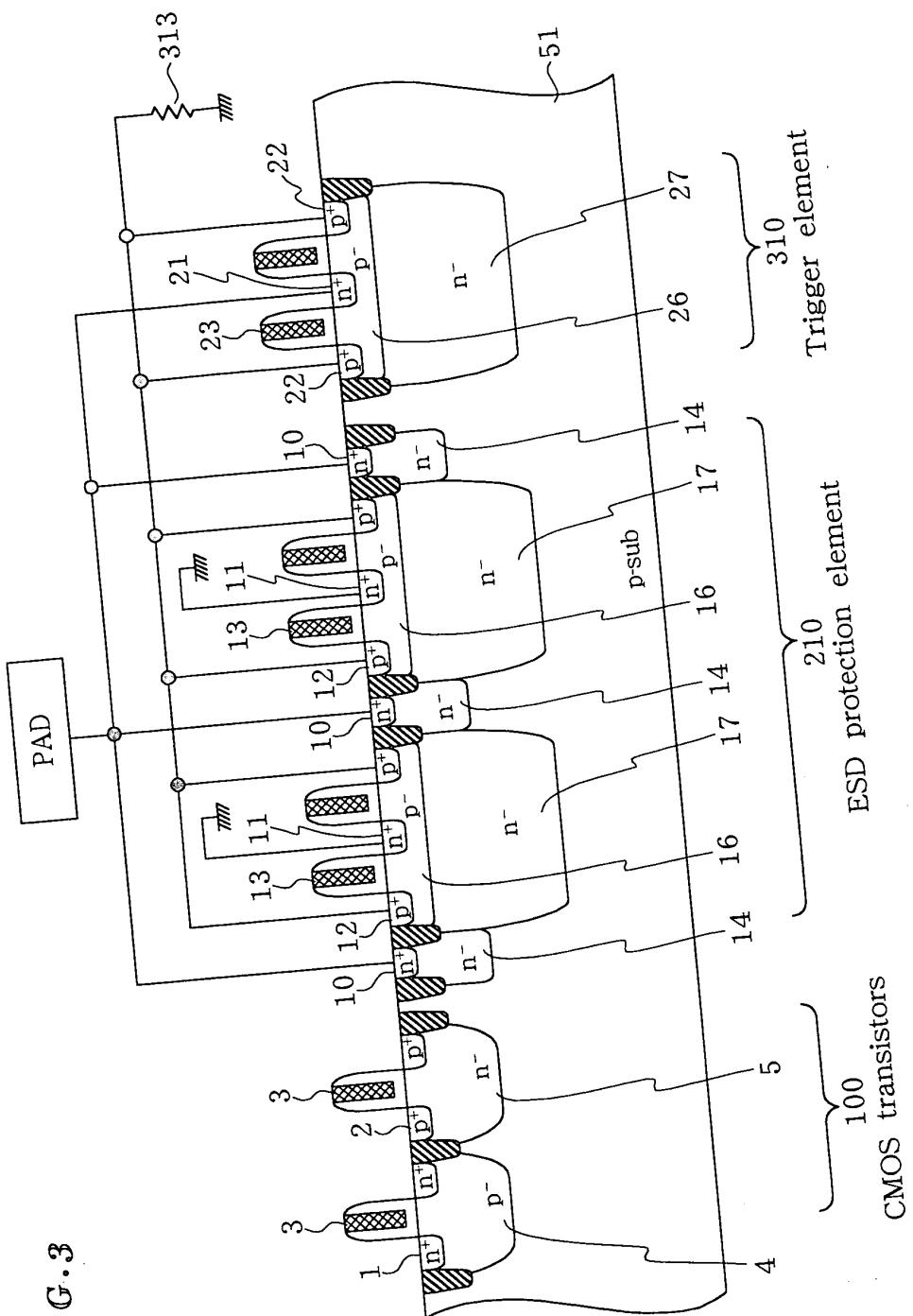


FIG. 4

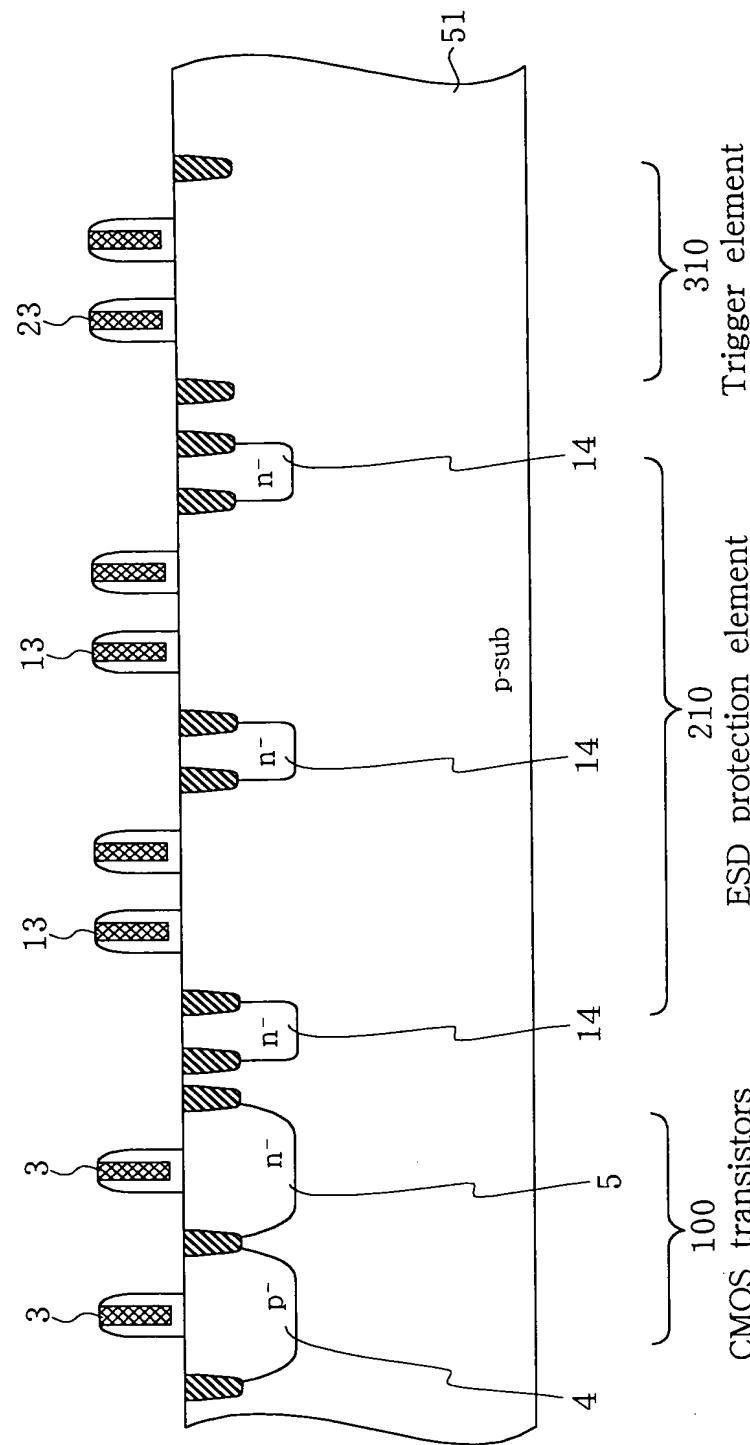
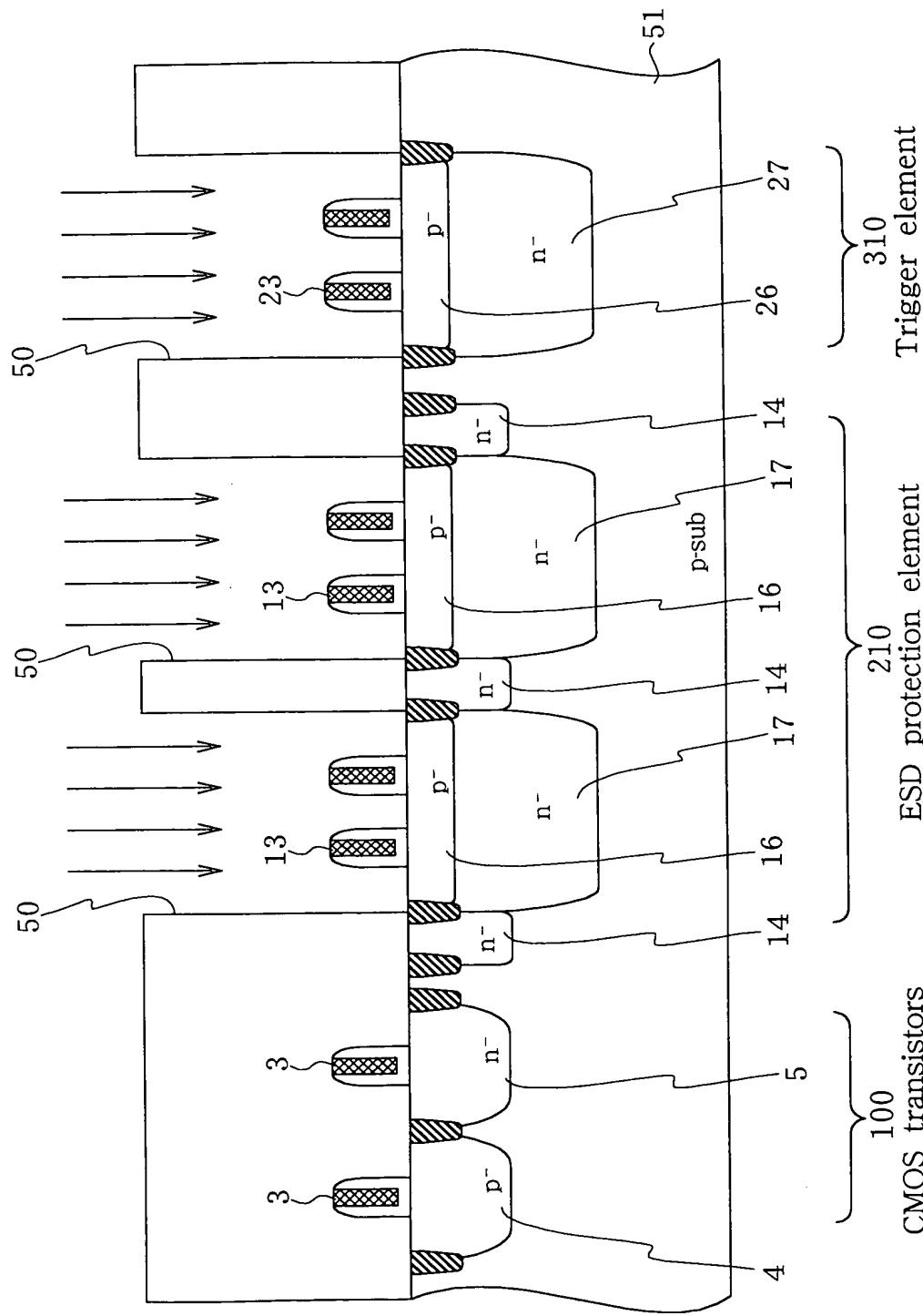


FIG. 5



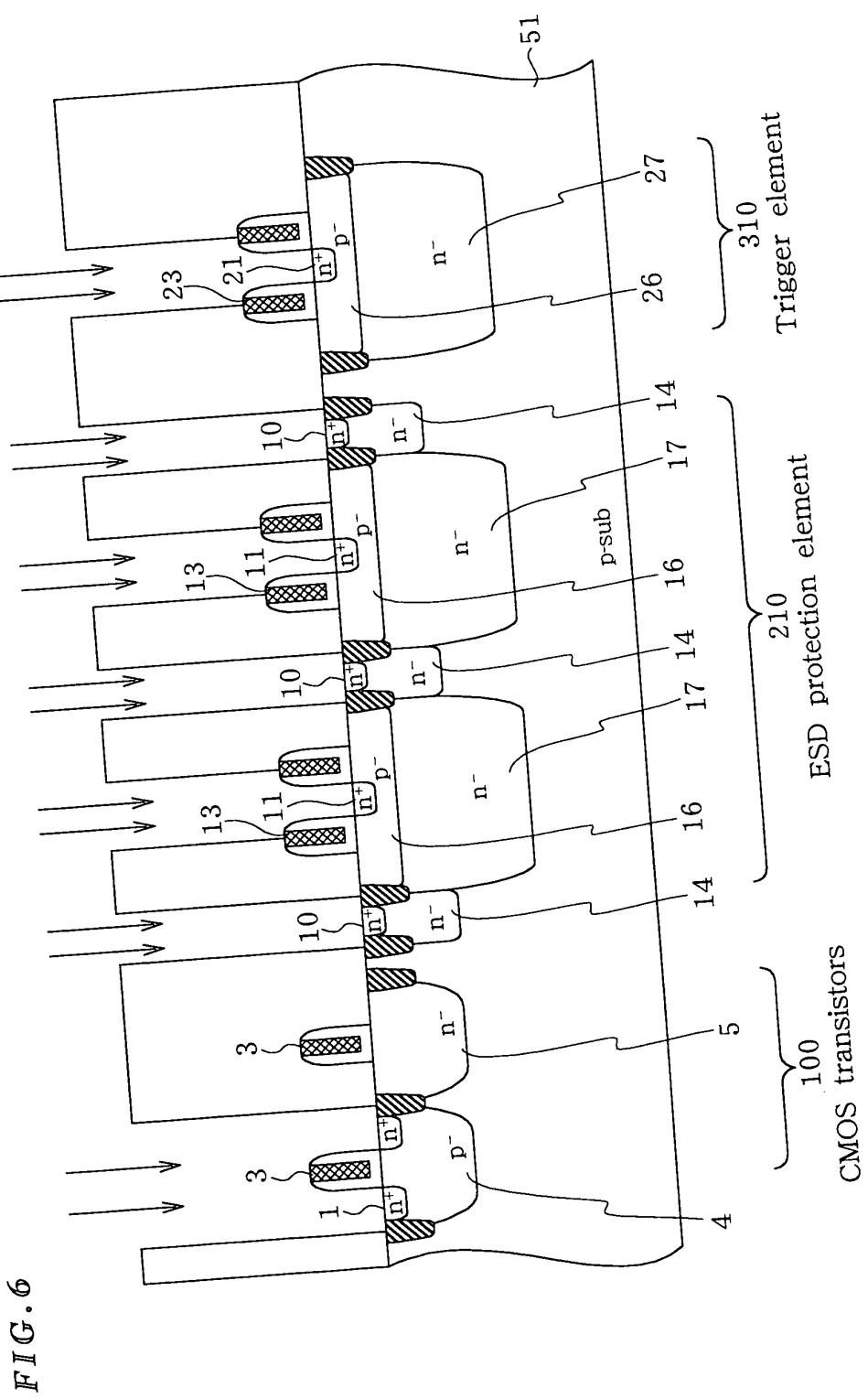
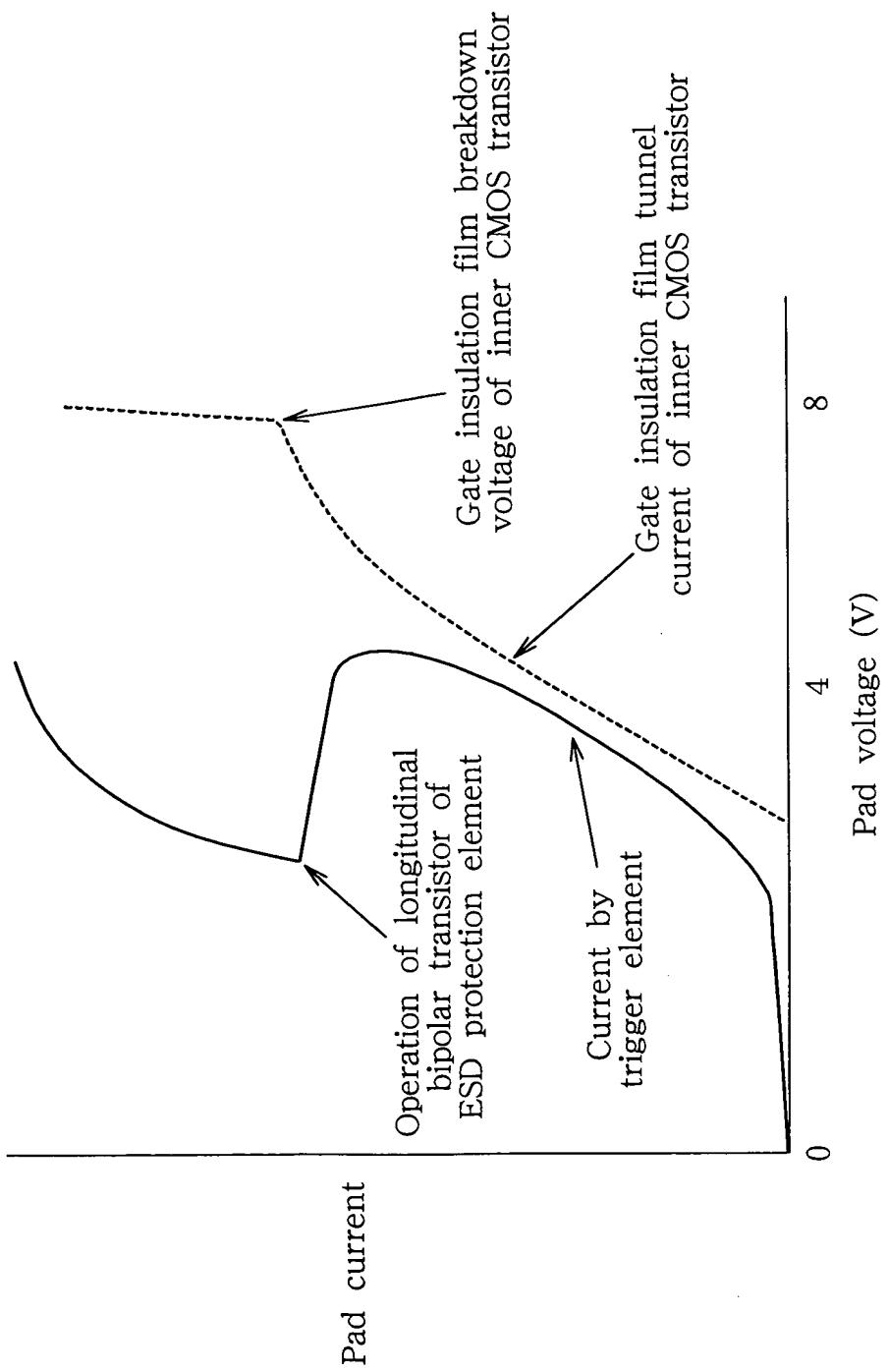


FIG.7

Operation voltage of longitudinal bipolar transistor < gate insulation film breakdown voltage of inner CMOS transistor

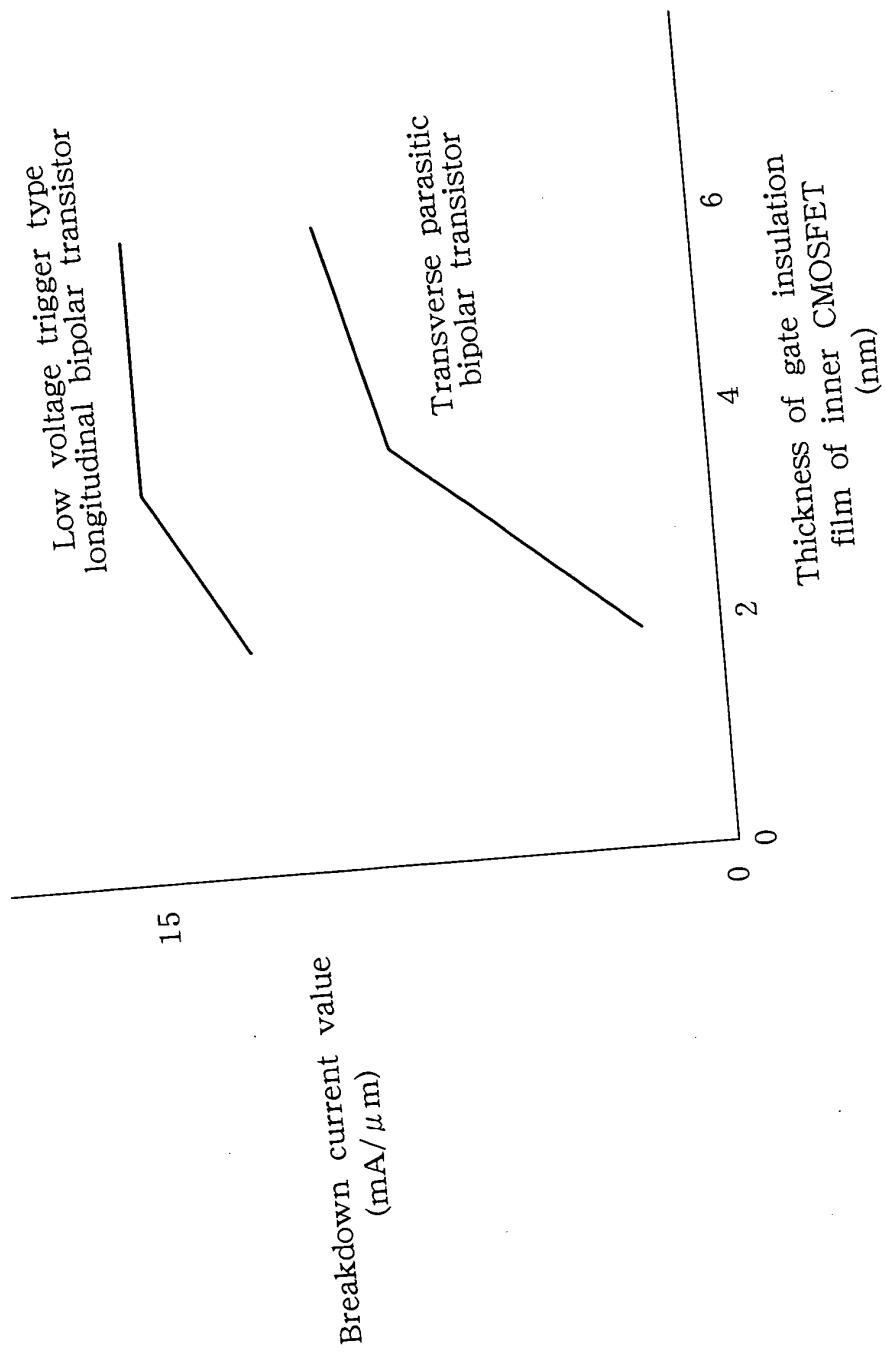
FIG. 8

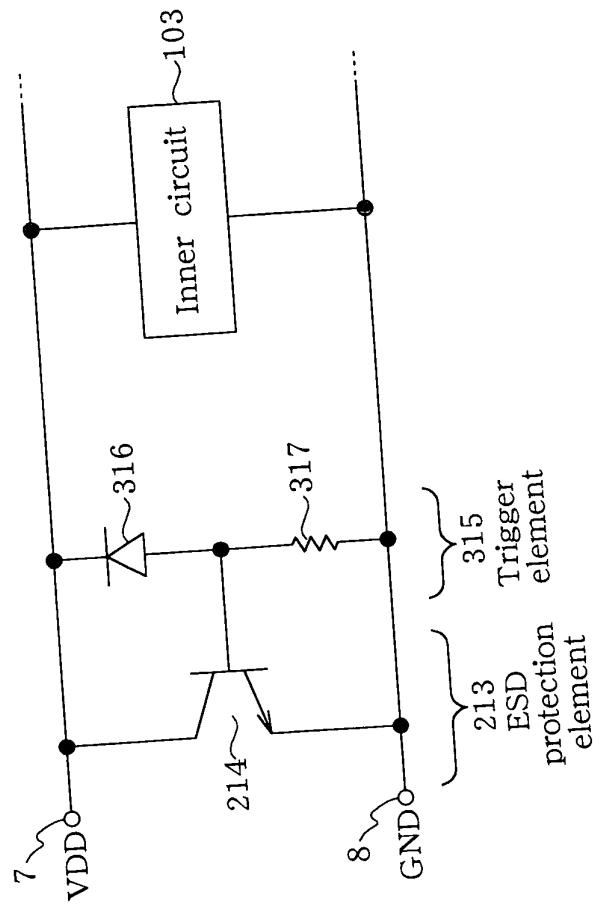
FIG. 9

FIG. 10

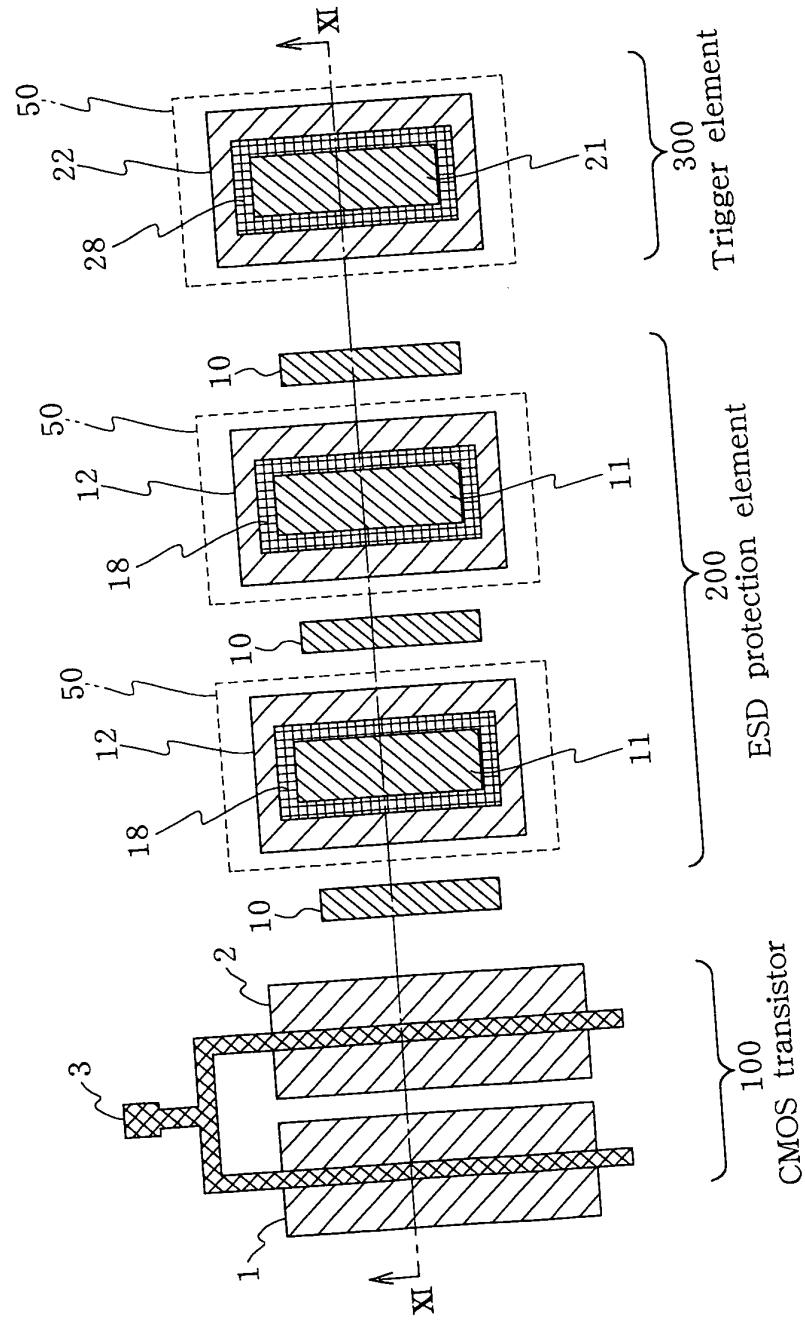


FIG. 11

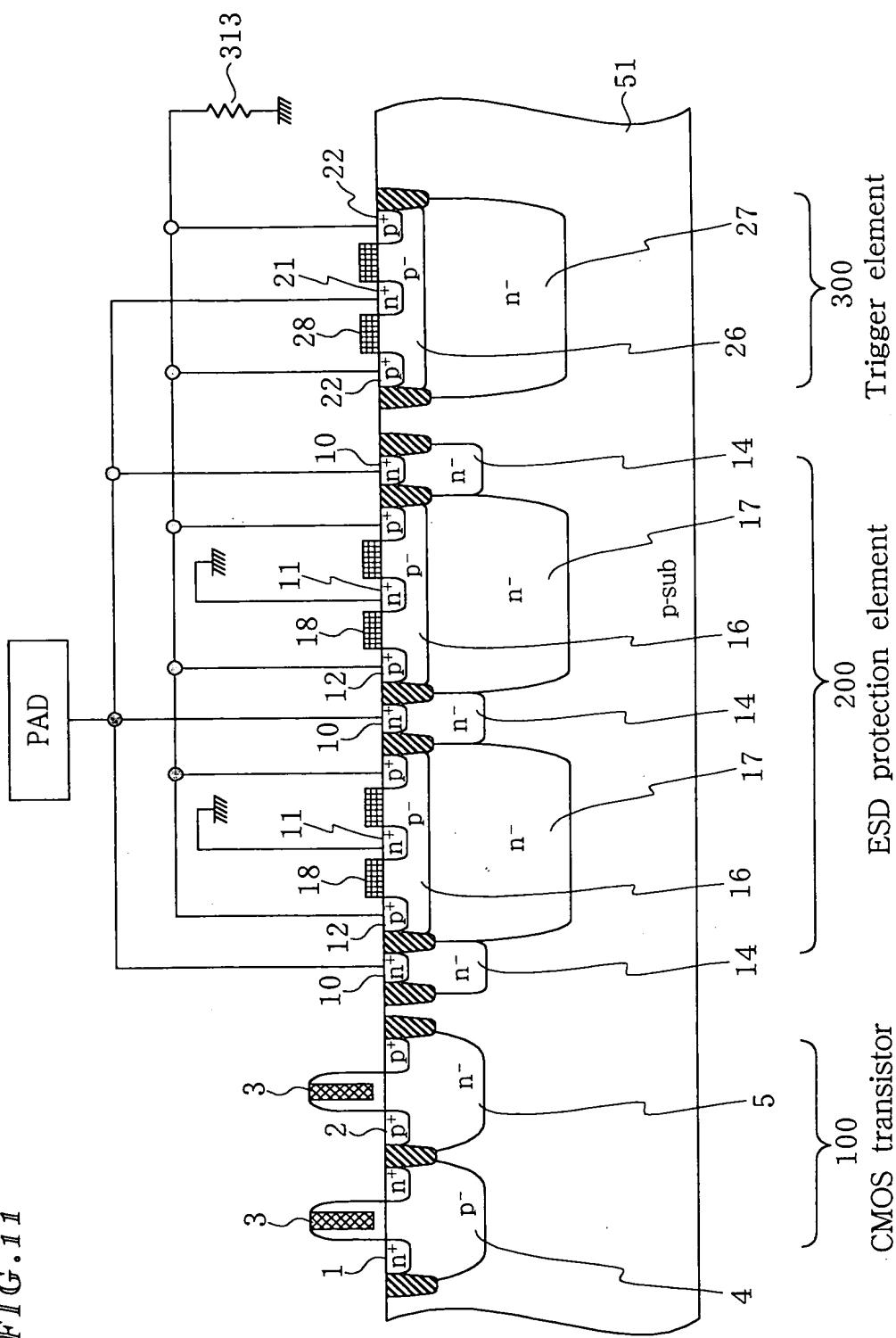


FIG. 12

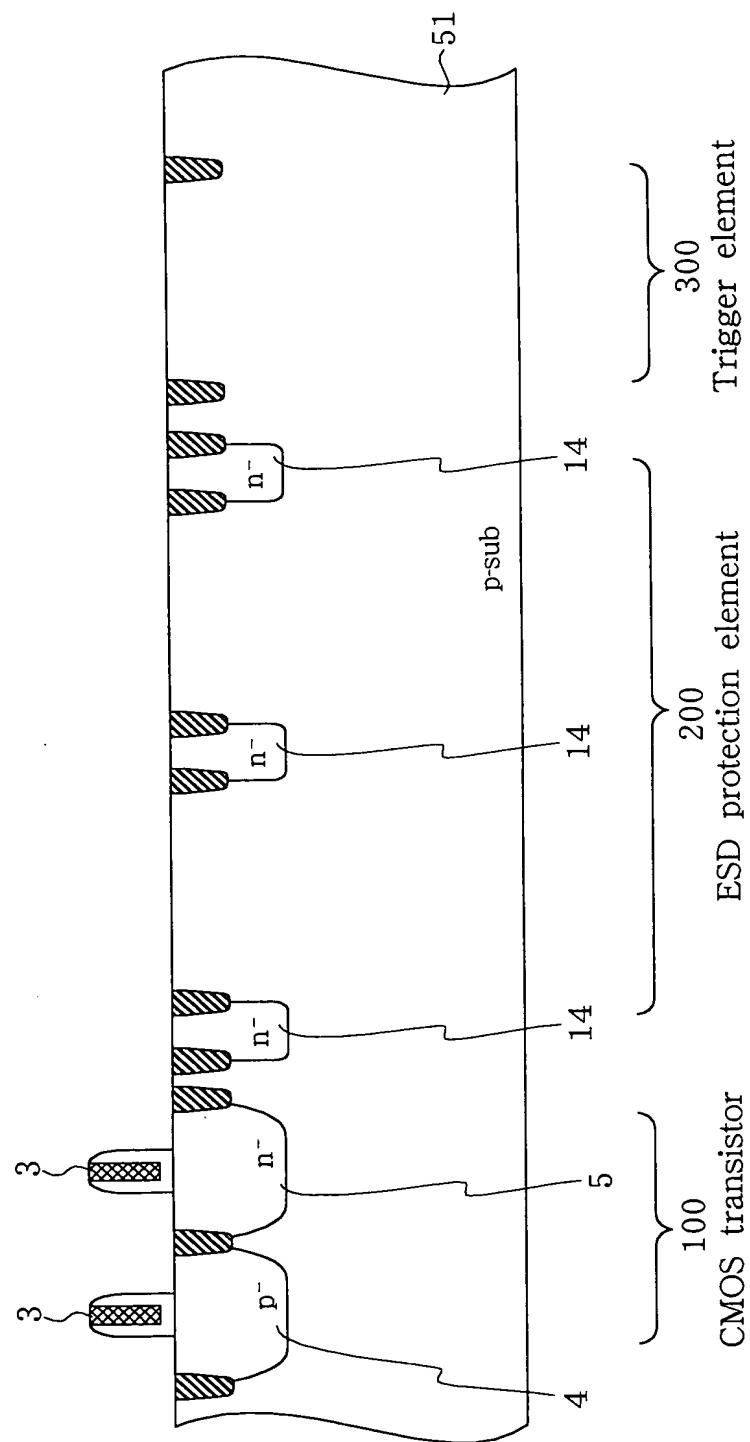


FIG. 13

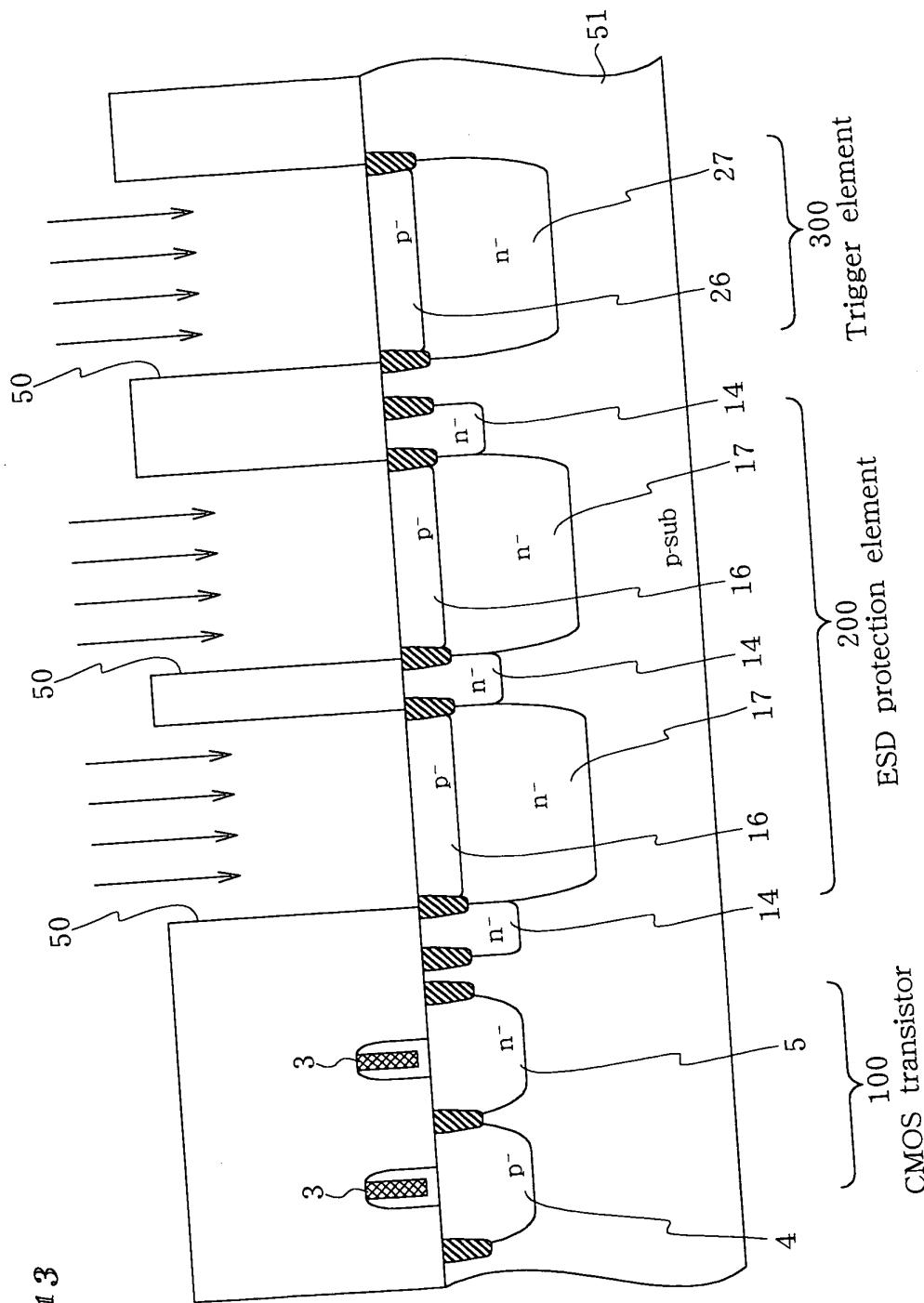


FIG. 14

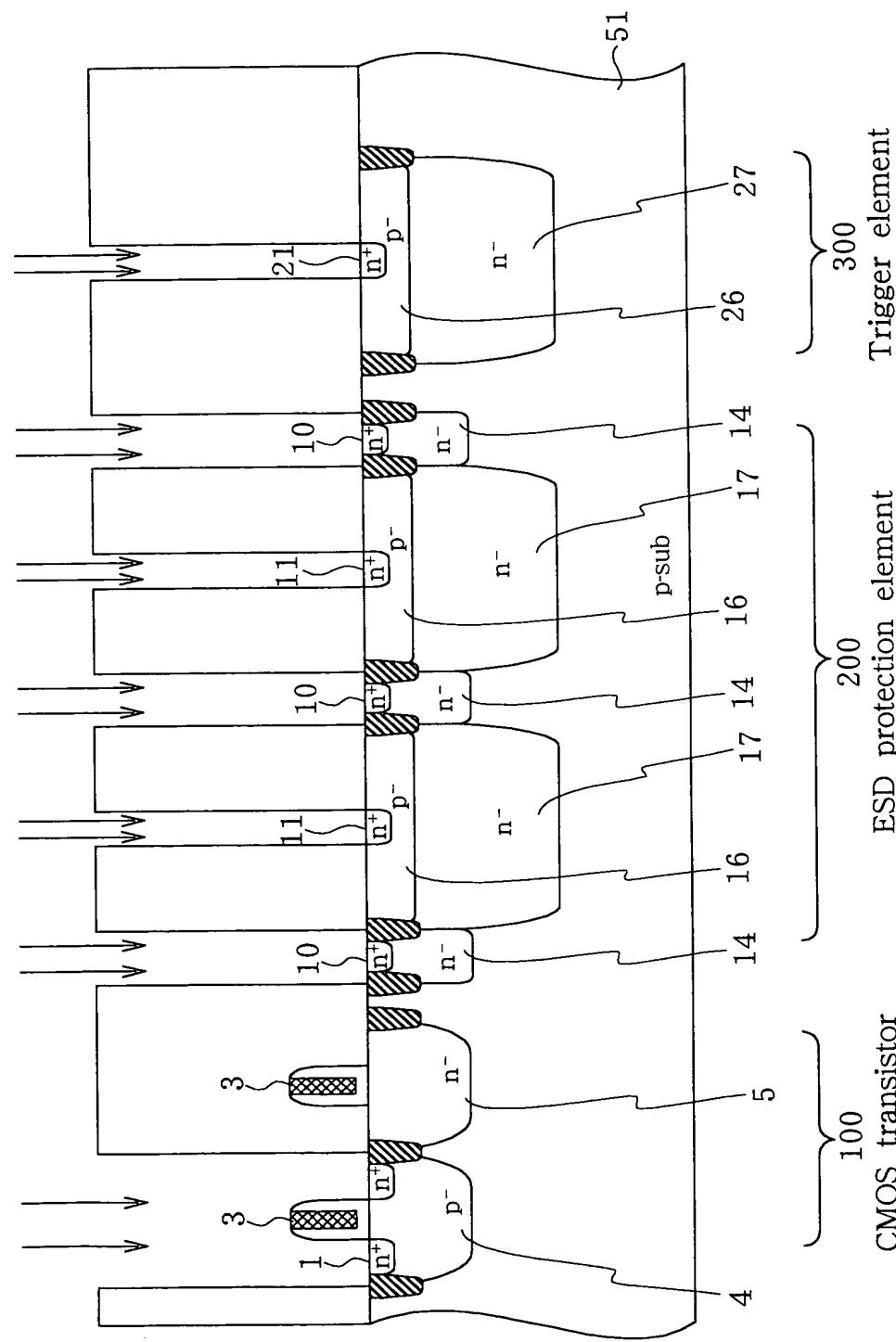
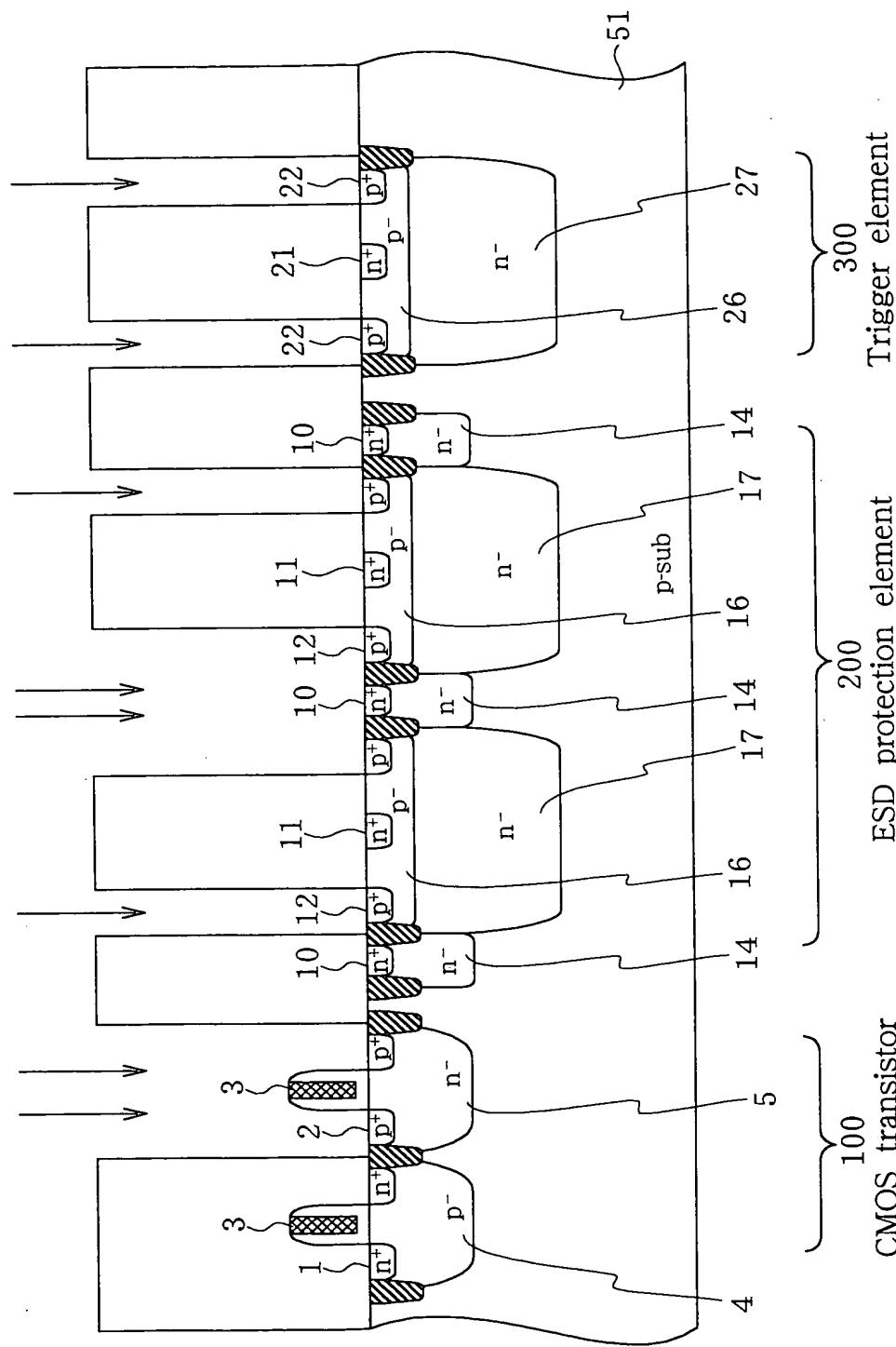


FIG. 15



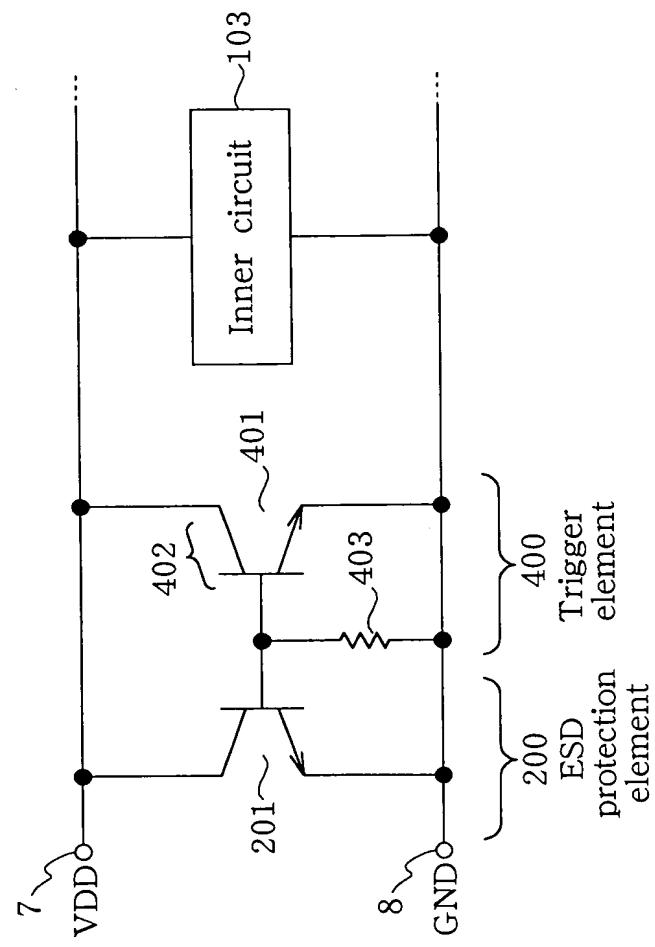


FIG. 16

FIG. 17

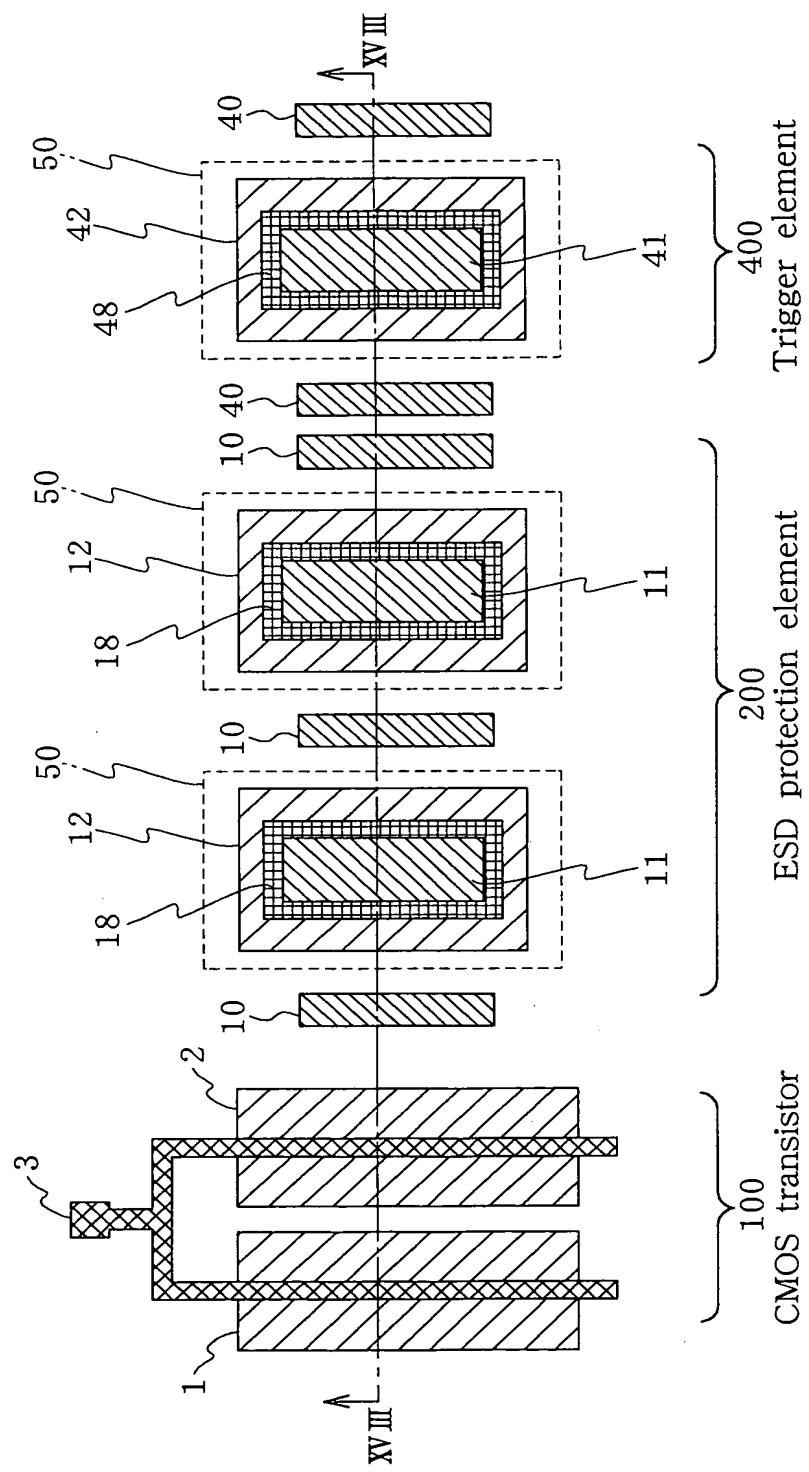


FIG. 18

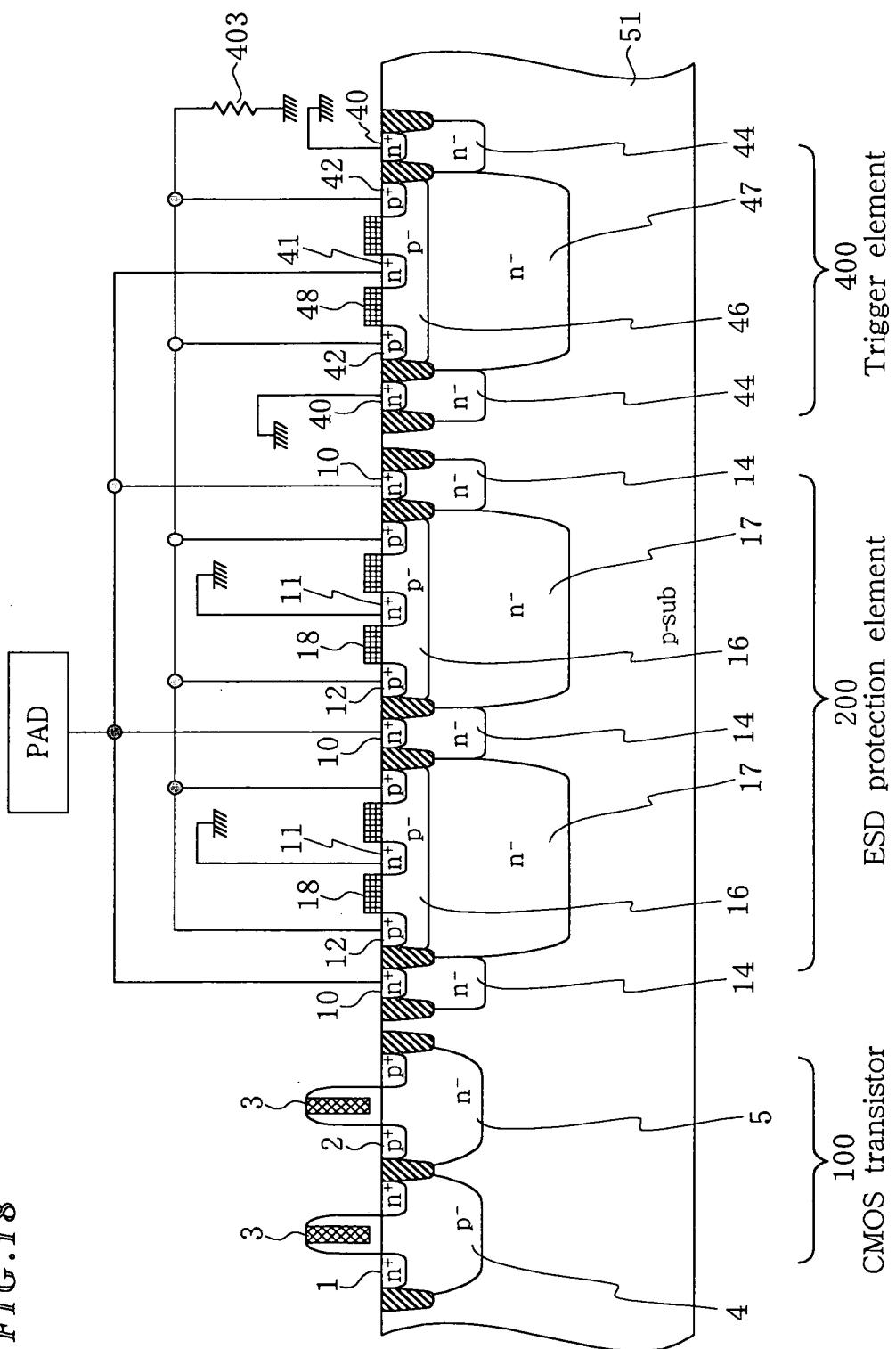


FIG. 19

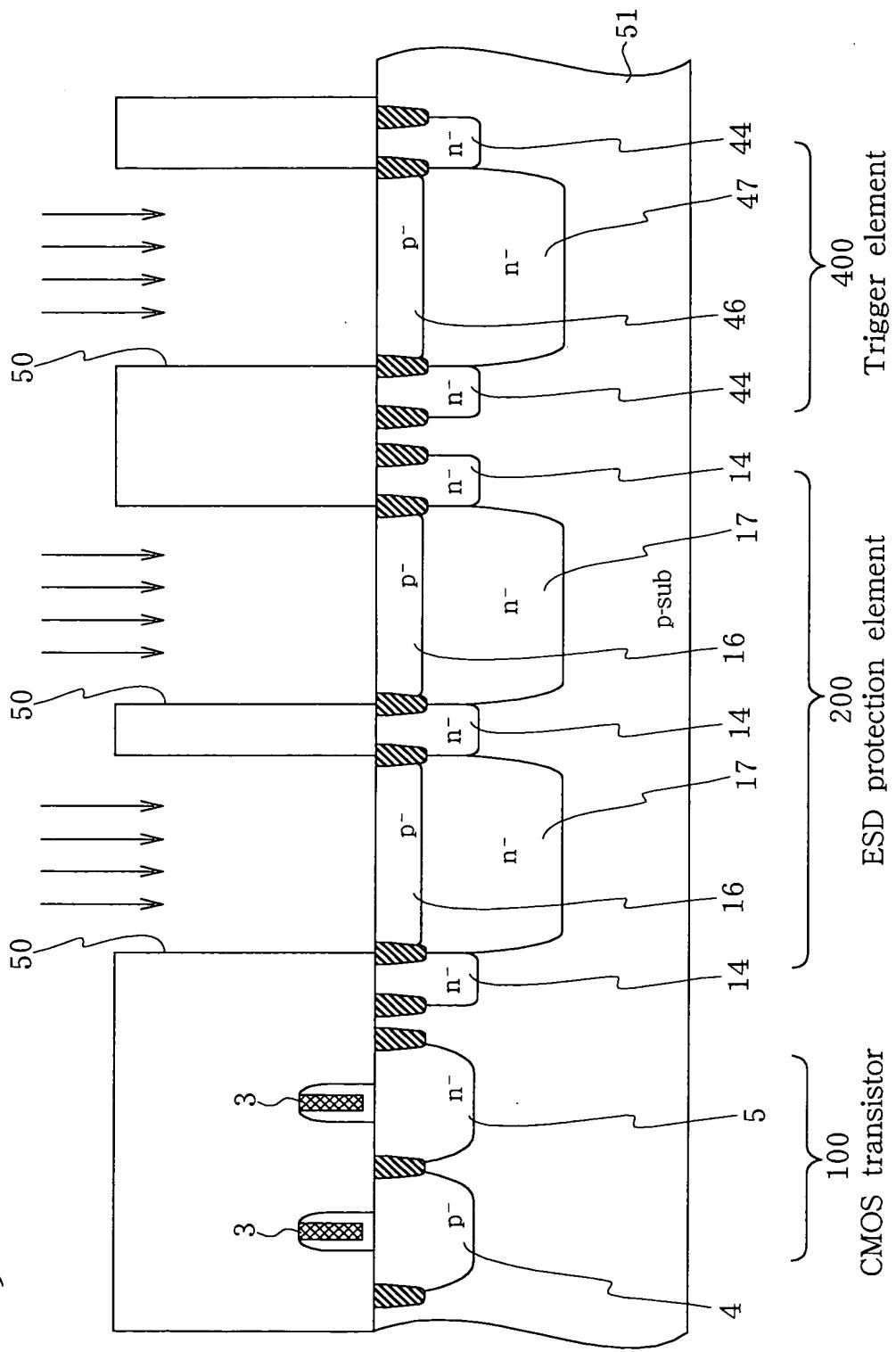


FIG. 20

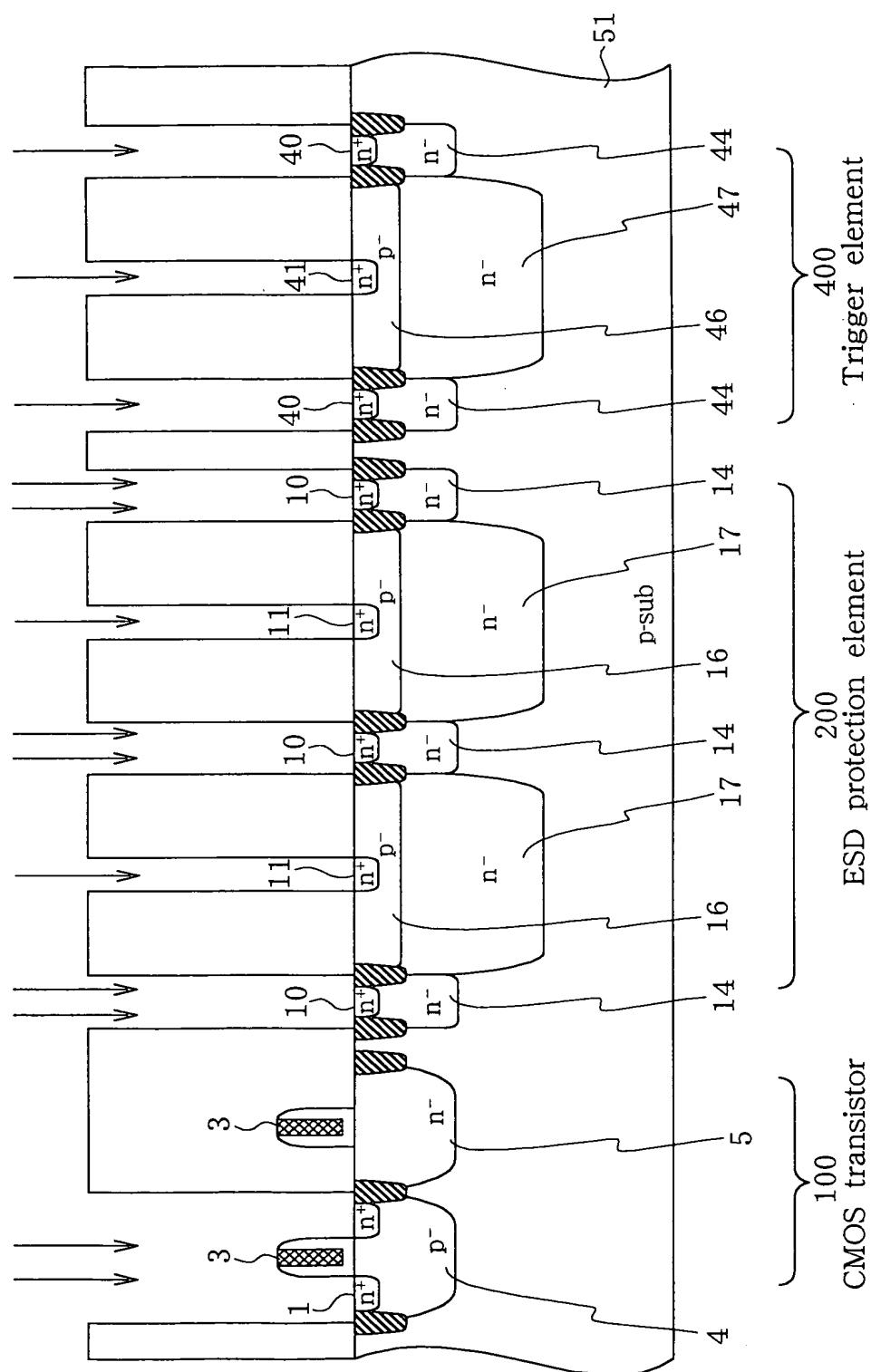


FIG. 21

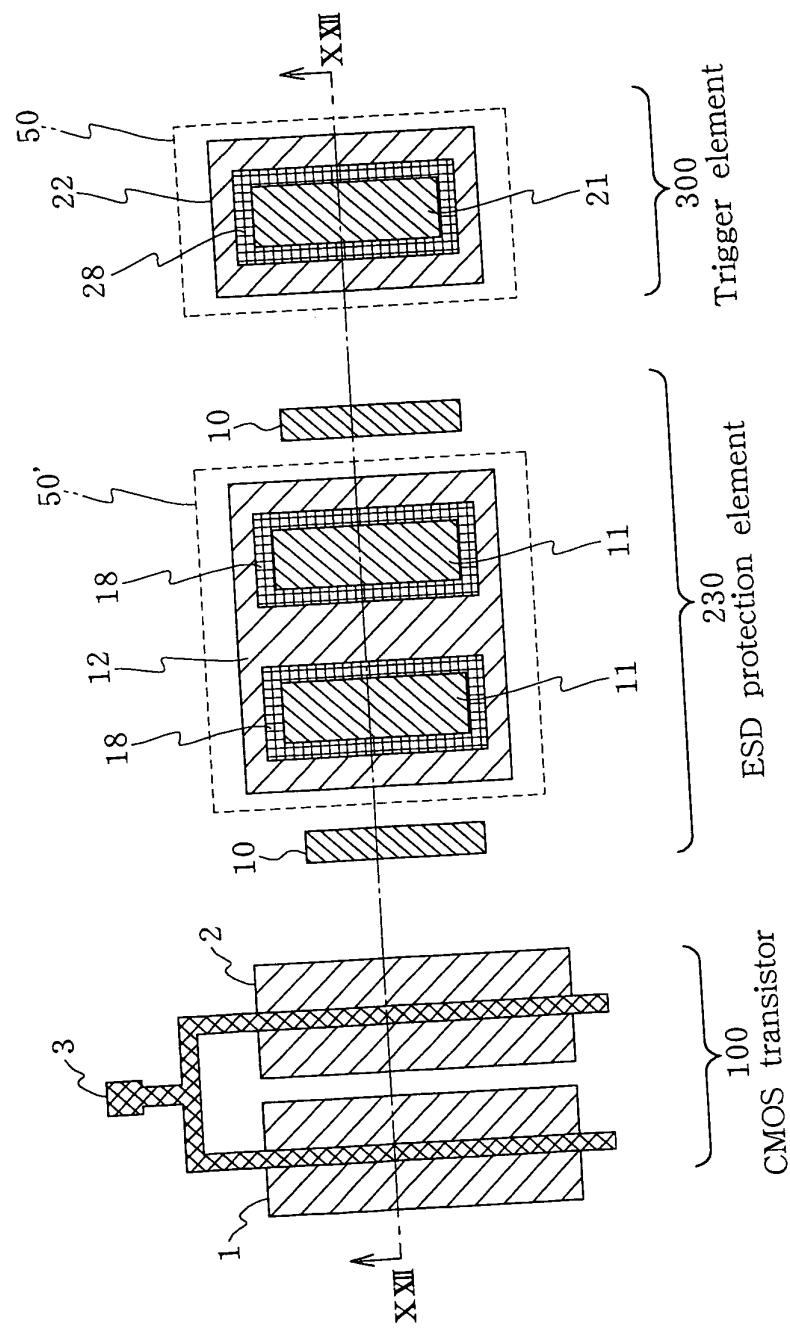


FIG. 22

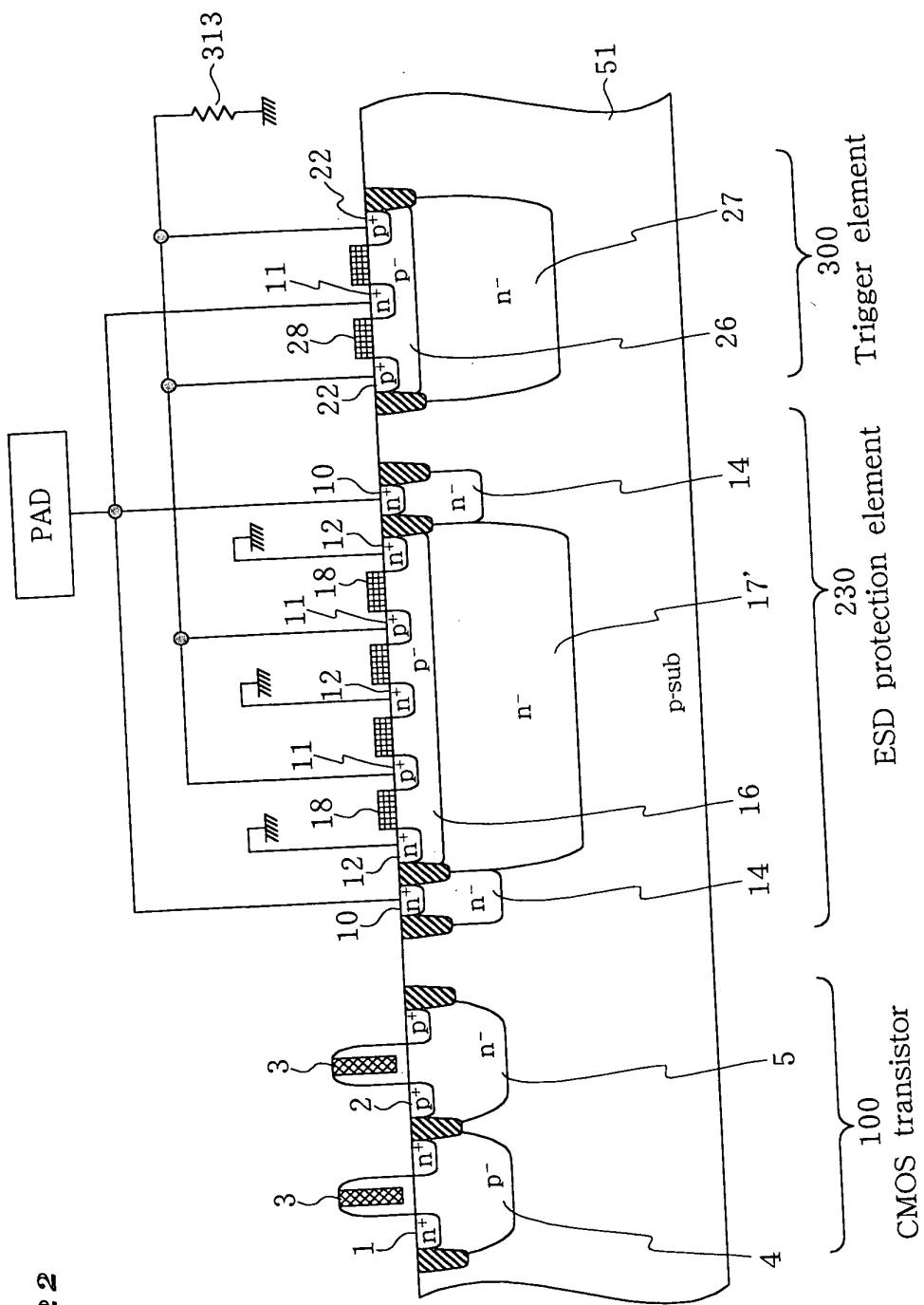


FIG. 23

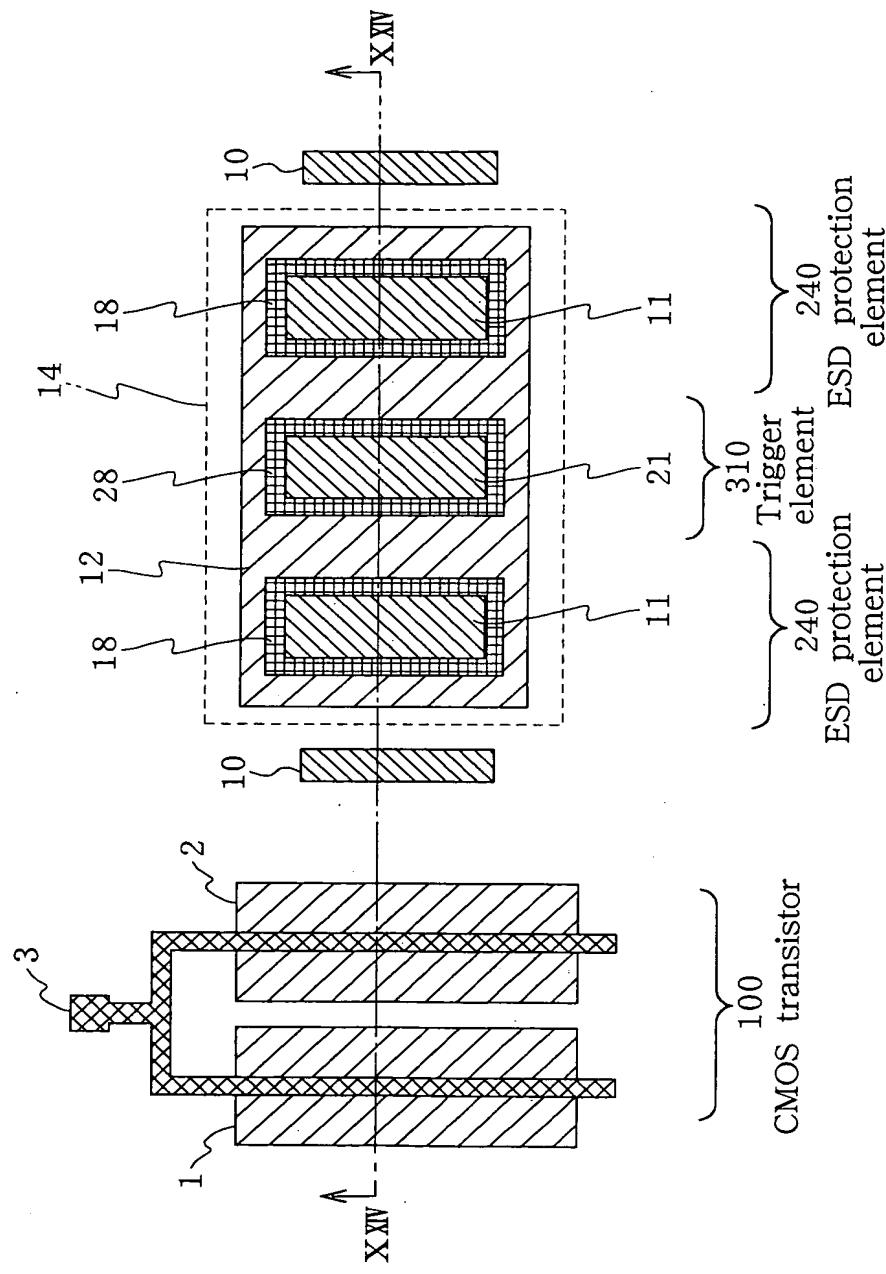


FIG. 24

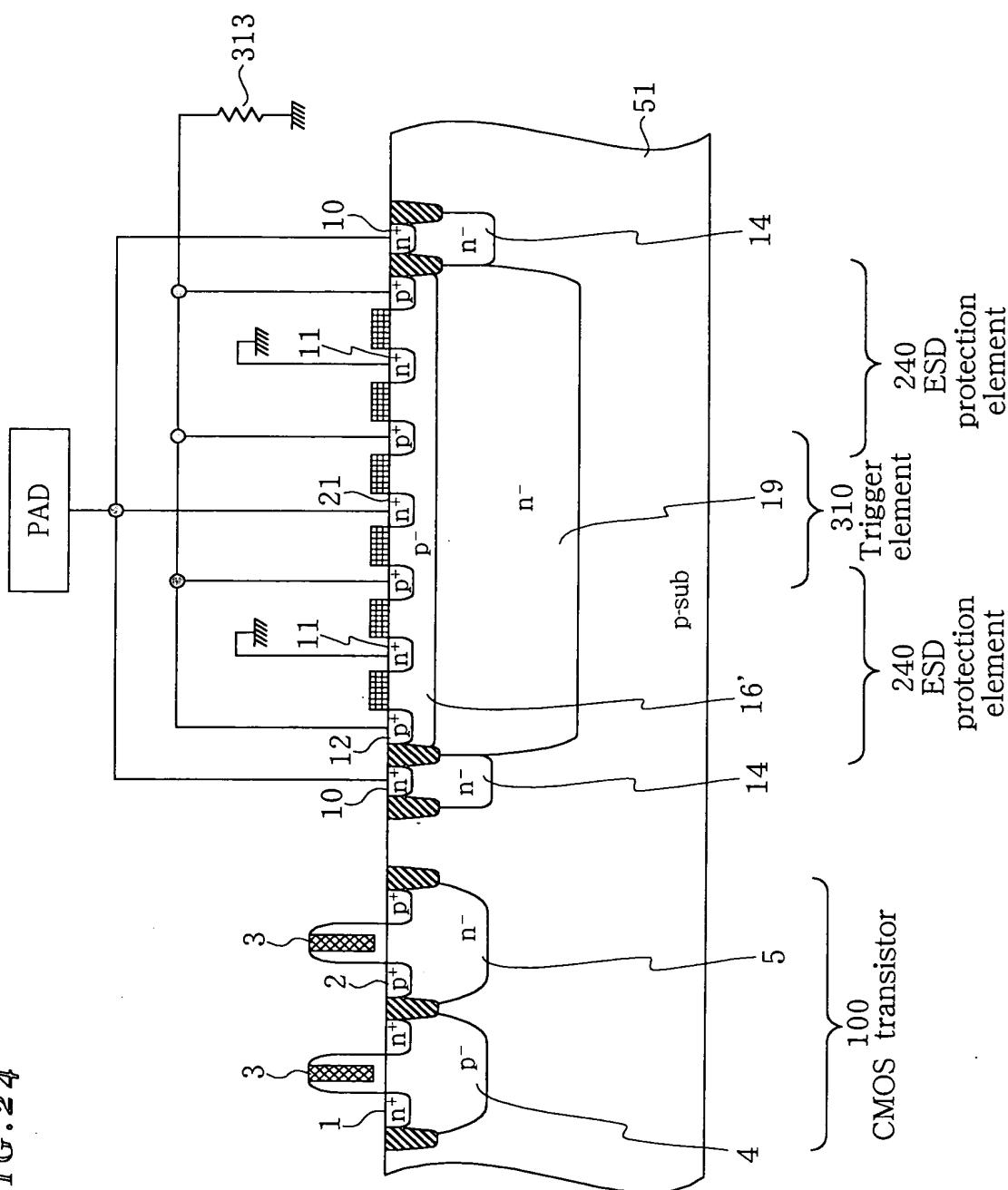


FIG. 25

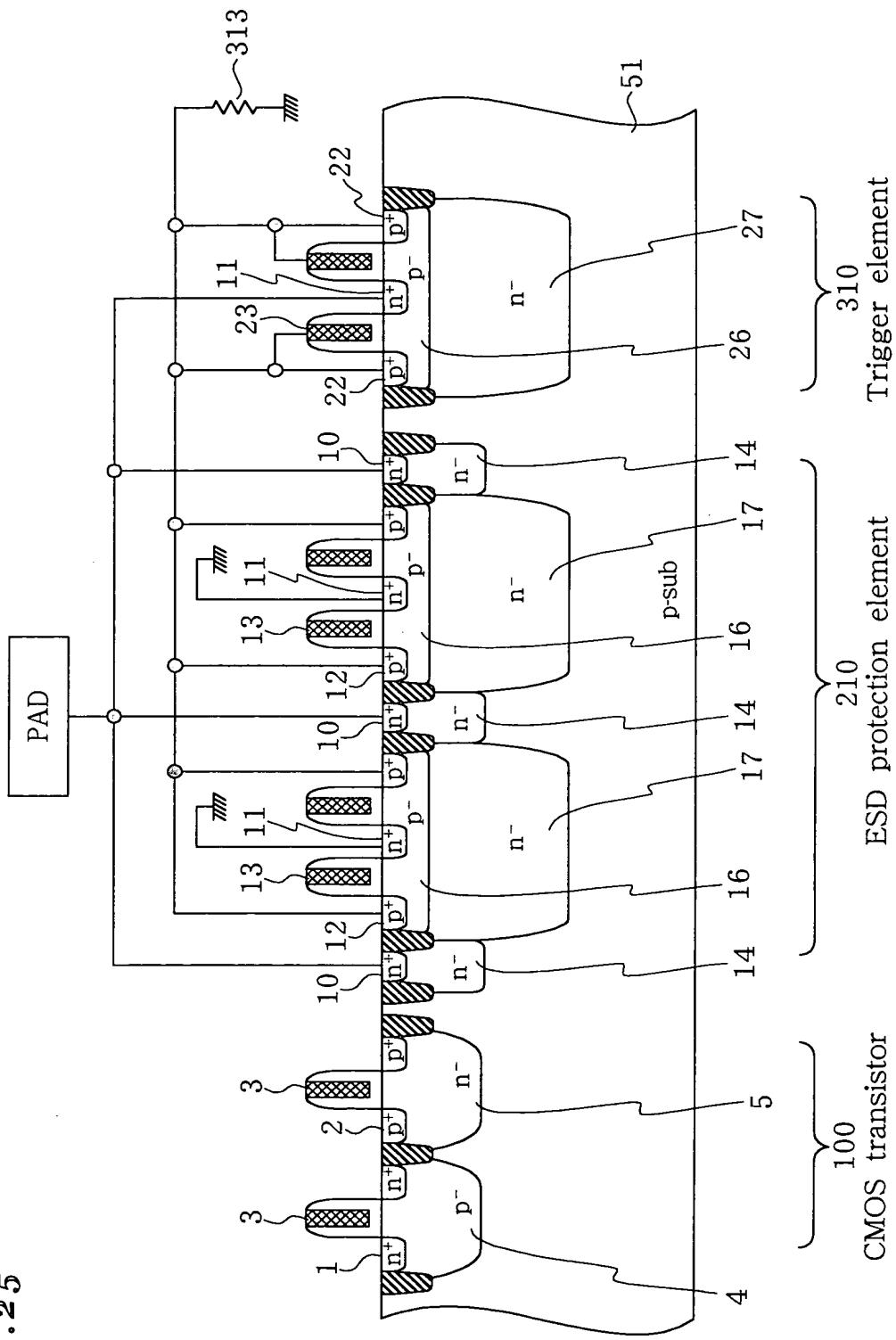


FIG. 26

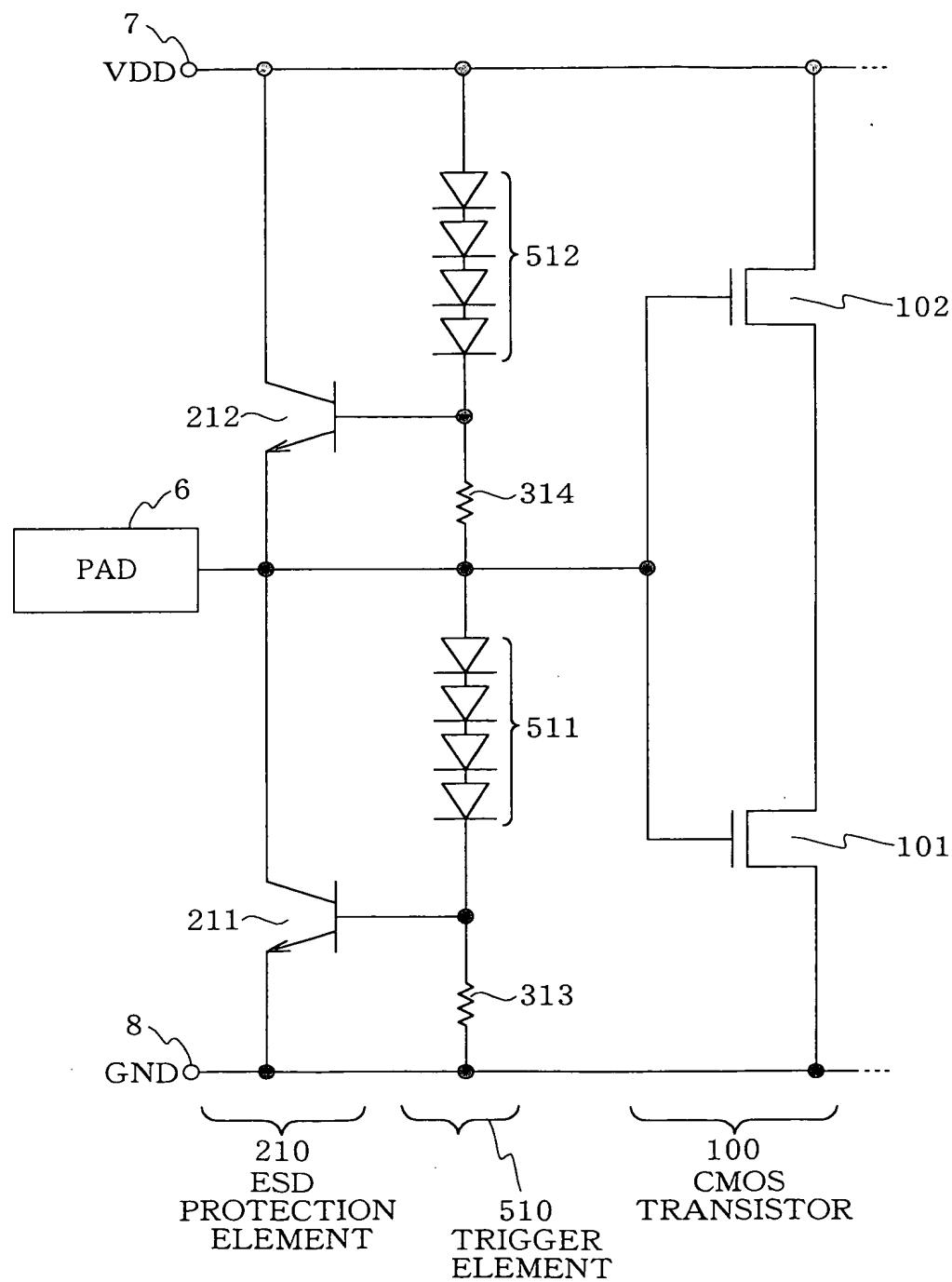


FIG.27

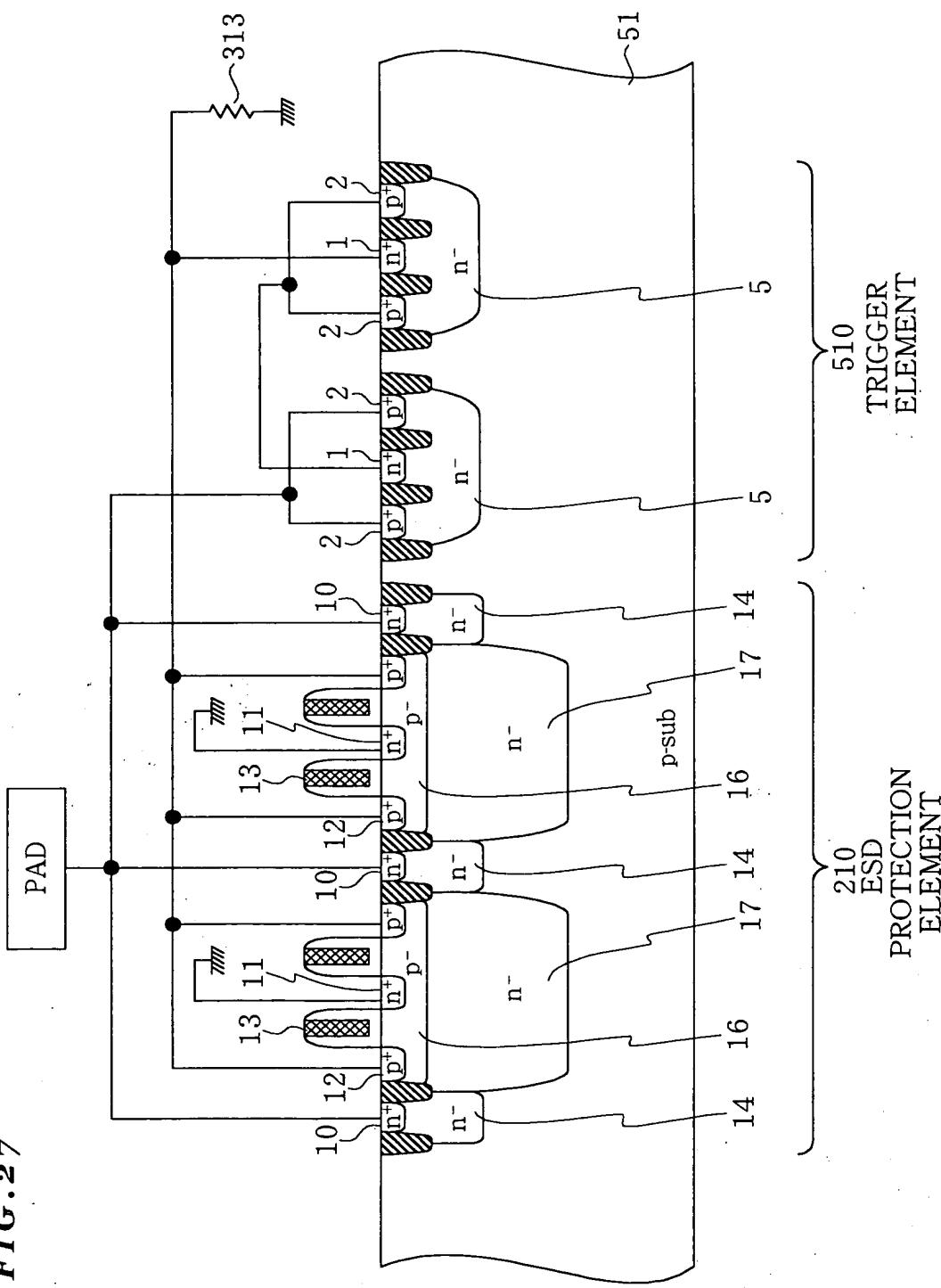


FIG. 28

**COMPARISON OF FORWARD SERIES CONNECTION DIODE
AND INVERSE DIODE**

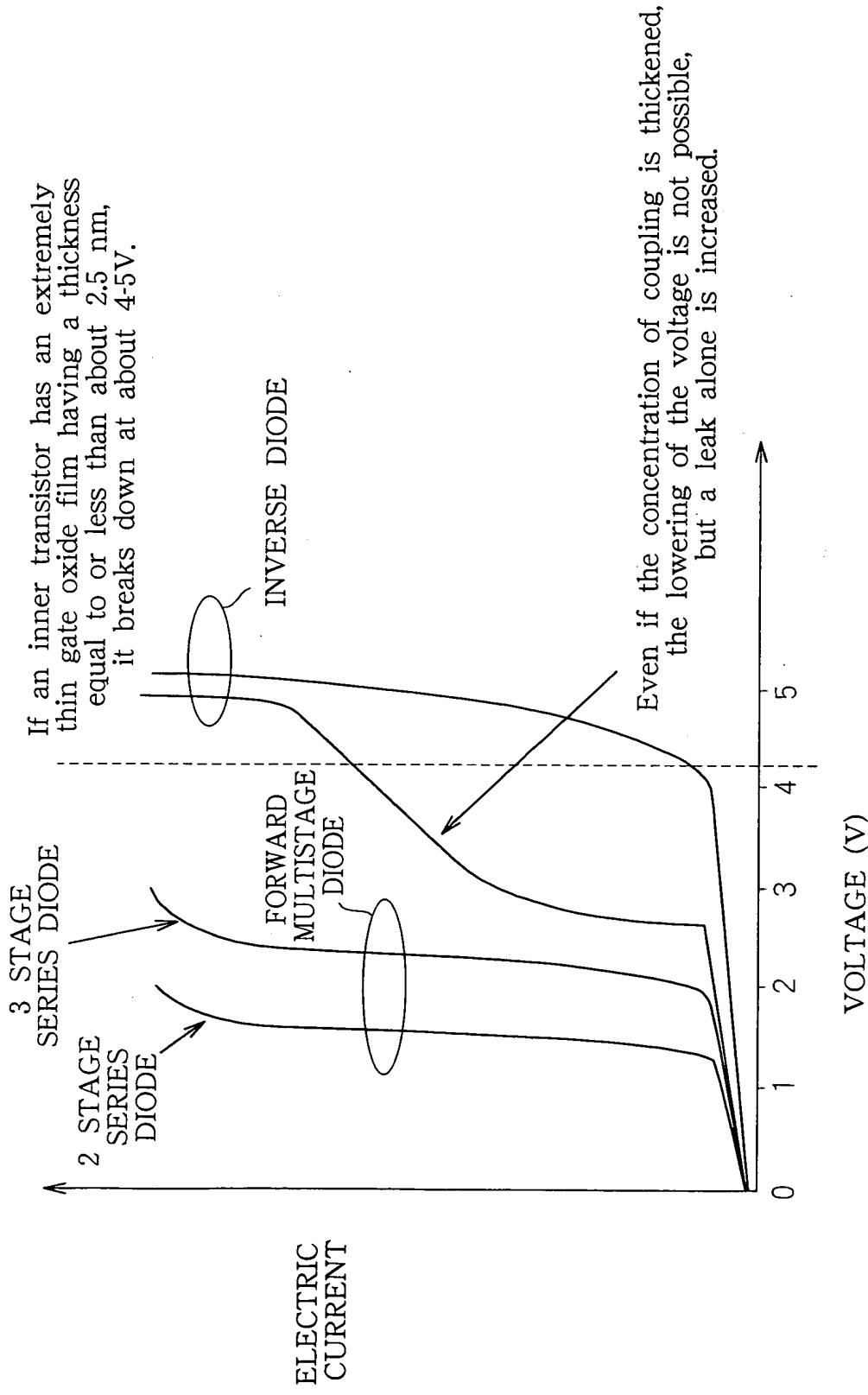
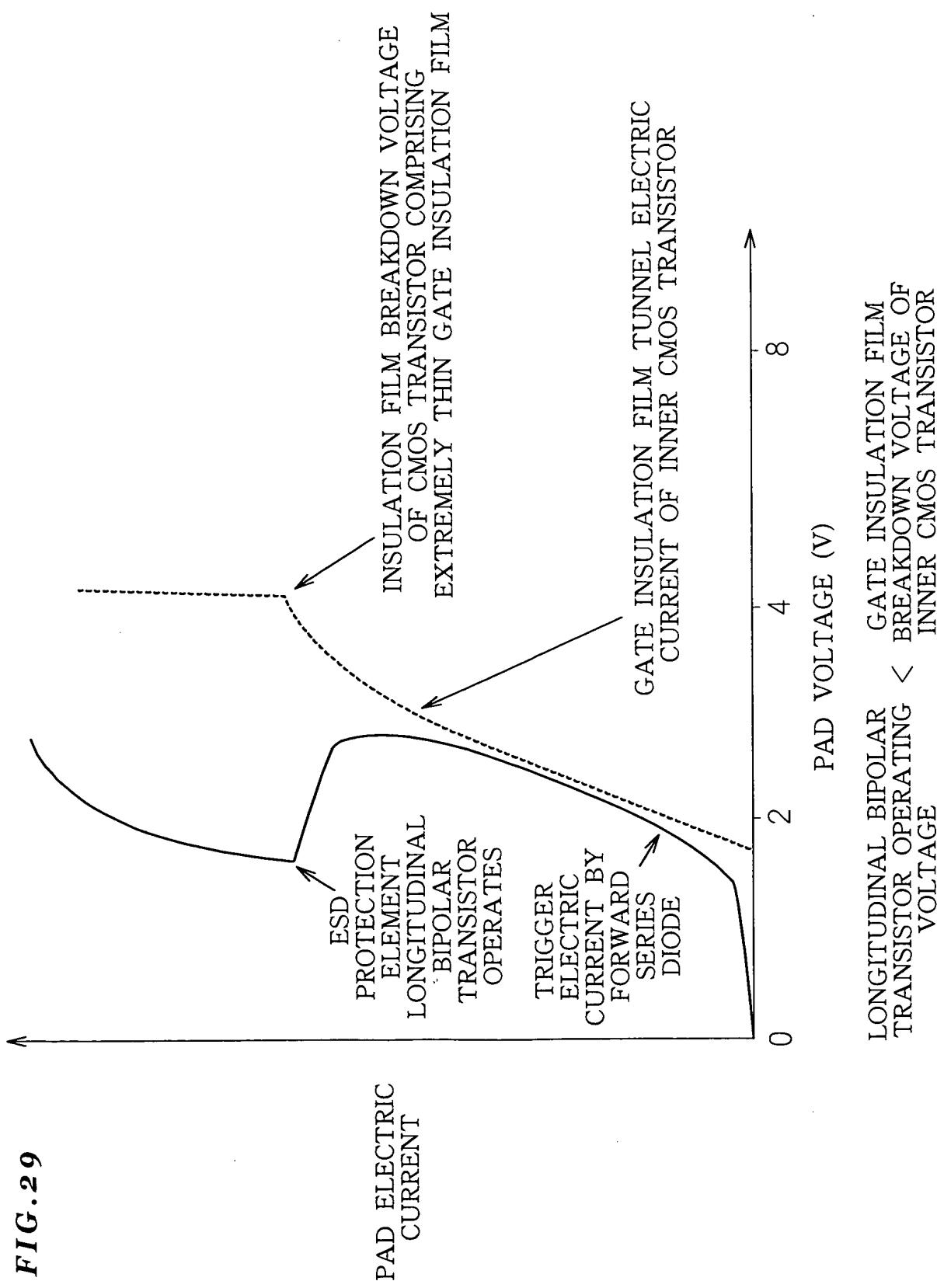


FIG. 29

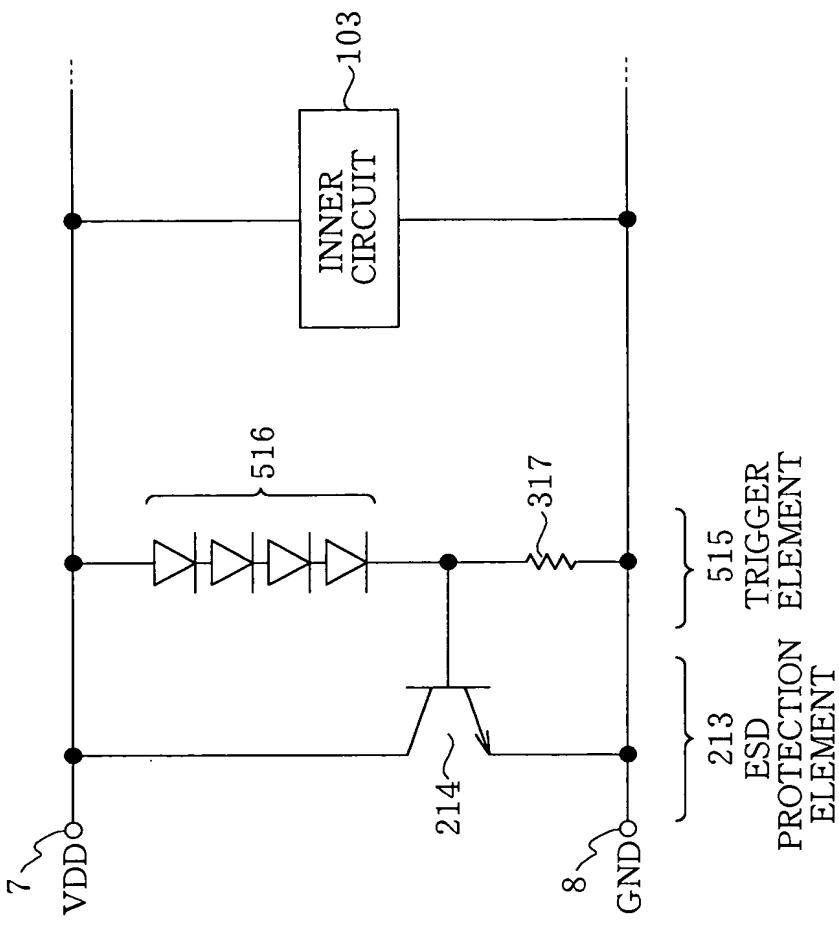


FIG. 30

FIG. 31

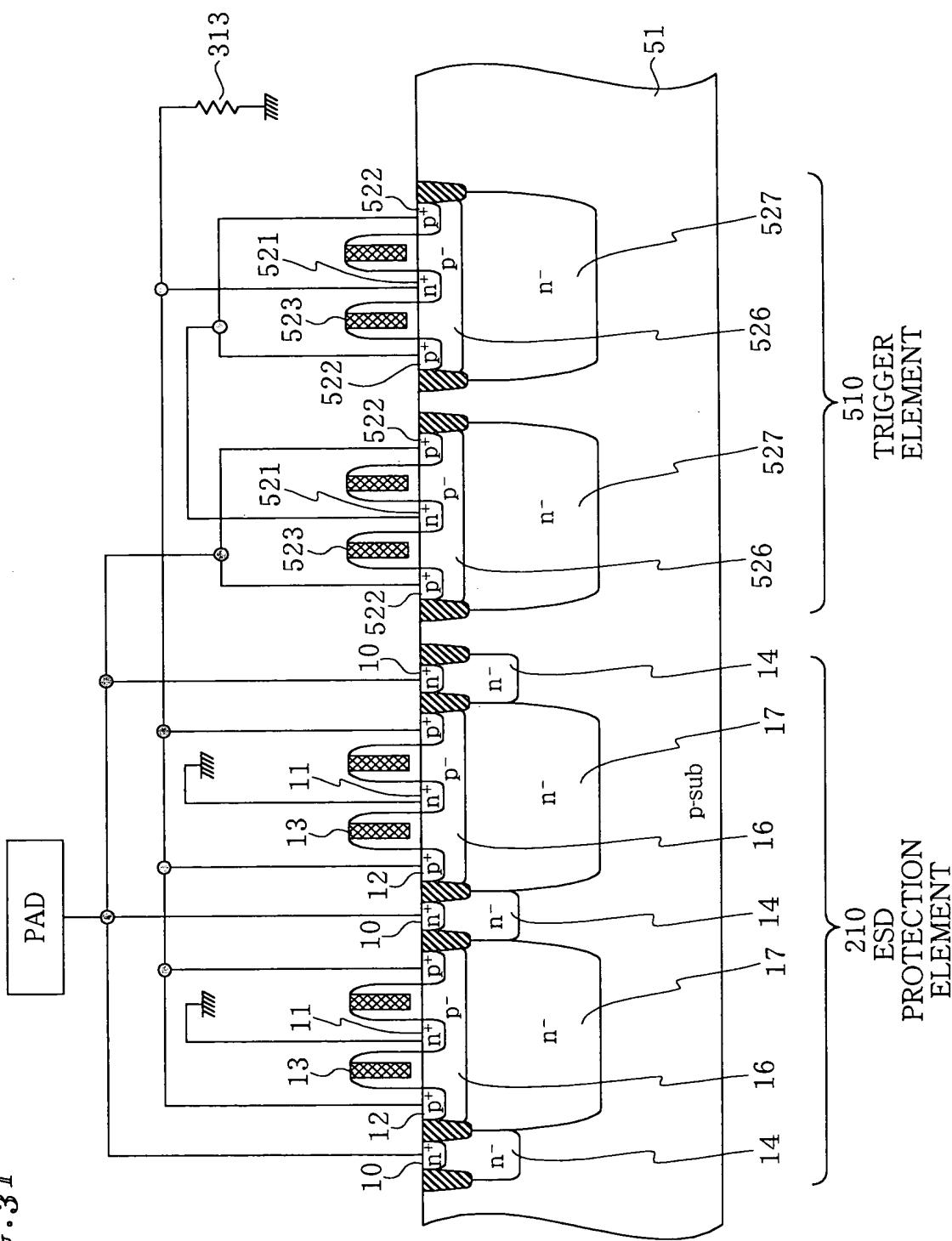
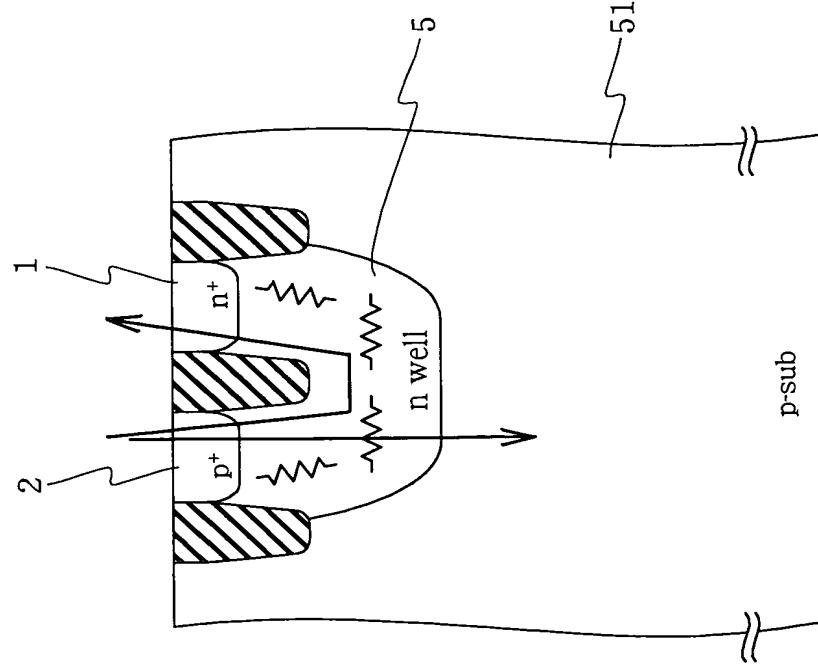


FIG. 32(a)

DIODE COMPRISING
p+LAYER/n well
FABRICATED BY
EXISTING CMOS PROCESS

**FIG. 32(b)**

DIODE UTILIZING ONE PORTION
OF LONGITUDINAL
BIPOLAR TRANSISTOR

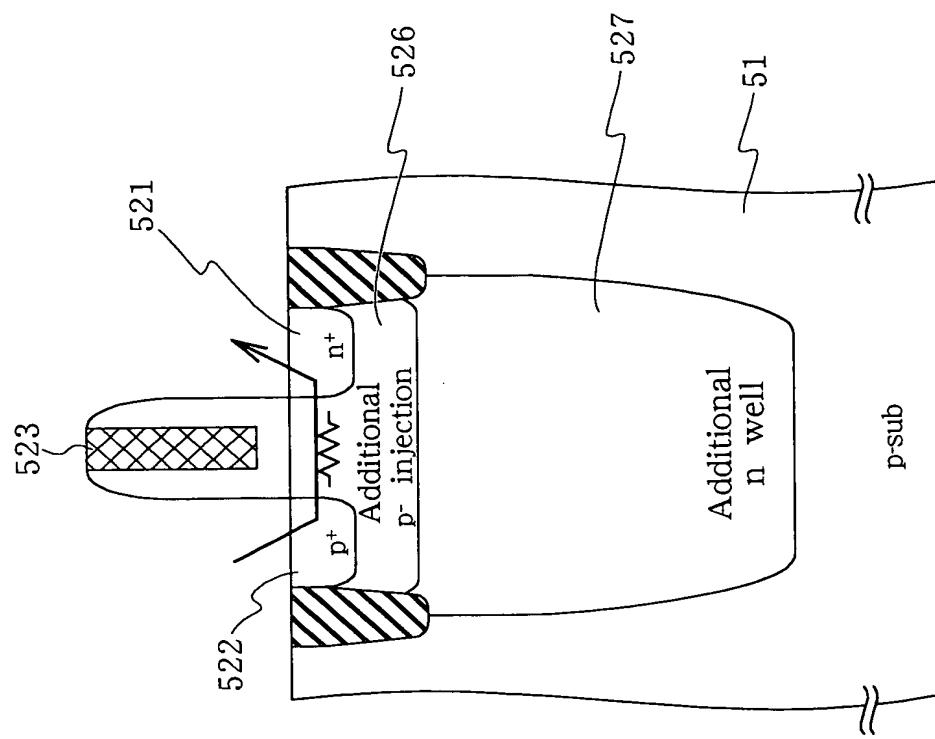
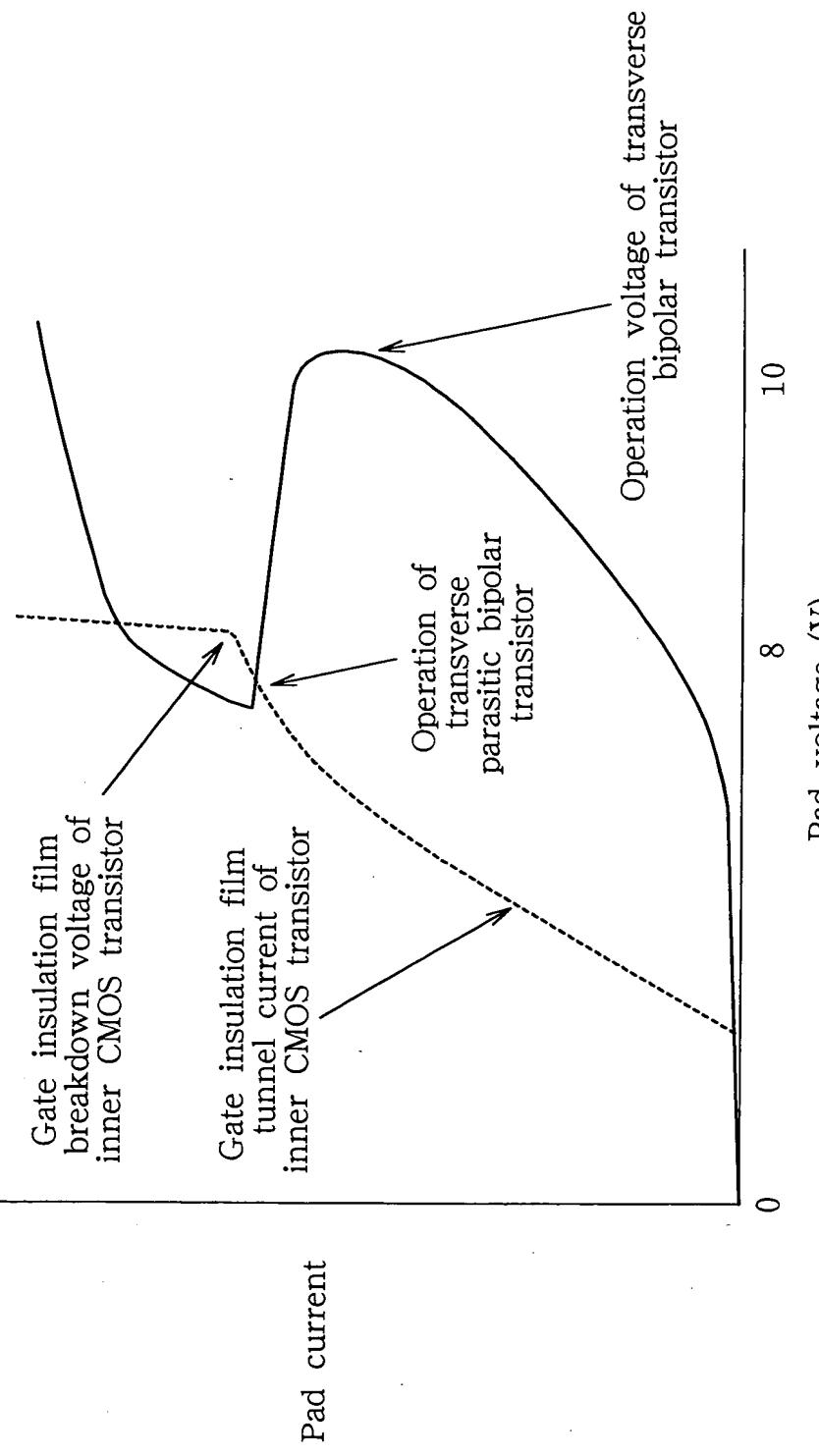


FIG.33

Operation voltage of transverse bipolar transistor < gate insulation film breakdown voltage of inner CMOS transistor